Developing a leading practical application for 3D IC chip stacking technology

— How to progress from fundamental technology to application technology —

Masahiro AOYAGI[1*], Fumito IMURA[1], Fumiki KATO[1], Katsuya KIKUCHI[1], Naoya WATANABE[1], Motohiro SUZUKI[1], Hiroshi NAKAGAWA[1], Yoshikuni OKADA[1], Tokihiko YOKOSHIMA[2], Yasuhiro YAMAJI[1], Shunsuke NEMOTO[1], Tung Thanh BUI[1] and Samson MELAMED[1]

[Translation from *Synthesiology*, Vol.9, No.1, p.1-14 (2016)]

3D IC chip stacking technology, which is a technology to vertically stack multiple IC chips such as CMOS, MEMS and power IC chips, is expected to be one of future electronic device integration technologies, because integration along the additional vertical dimension affords efficient use of space and innovation of system architecture. We developed fundamental technology of high density integration for 3D IC chip stacking. To accelerate industrial applications of this technology, a mass-production process was developed in collaboration with a manufacturing equipment company.

Keywords : Semiconductor device, IC, 3D stacking, packaging, TSV

1 Introduction

The electronic devices that evolved using semiconductor integration devices as core parts were commercialized for use in industrial devices, home electronic devices, and personal mobile electronic devices, through continuous technological development for increased performances such as achievement of small-size packaging, high-density integration, and low power consumption. They have spread throughout businesses, households, and on a personal level, and dramatic increase in the number of products was seen worldwide. By the end of 2014, the diffusion rate exceeded 100 %, where the number of mobile phone holders became larger than the number of the world population.[1]

The innovation that should be brought to attention in the history of semiconductor integrated device is the achievement of tolerance to large manufacturing variation in the property of elements. Wide margin of operability was obtained compared to other device structures through the employment of complementary metal oxide semiconductor (CMOS) transistor device structure, where the n-channel and p-channel MOS transistors are paired together. This enabled the realization of an integrated circuit (IC) with over one billion transistors integrated on a chip.[2]

On the other hand, various limiting factors such as the size reduction limit of microfabrication and increased manufacturing costs became apparent for the semiconductor IC technologies, and the attempt to increase the integration density seemed to face the limit. The three-dimensional IC chip stacking technology whereby the IC devices are stacked vertically and packaged is one of the solutions, and expectation for it is rising recently as a technology for semiconductor device stacking that enables the increase of integration density for semiconductor ICs. Therefore, we established the fundamental technology for high-density high-integration electronic hardware construction required for 3D IC chip stacking, and we are working on the R&D of the application phase to create the flow of application system development, while engaging in technical support of mass-production technology that, in practice, should be undertaken by leading companies.

2 Advancement of electronic hardware system integration technology by 3D IC chip stacking and the goal of this research

First, we shall review the recent development trends of the electronic hardware system integration technology that advanced the manufacturing technology in response to the demand for high density and high integration to enhance the system performance. The system integration method called the system in package (SIP)[Term 1] is gaining attention, where several IC chips are stacked in a semiconductor IC package to integrate them into a certain size electronic system. This method enables stacking in the vertical direction that is different from the planar integration technology of

1. Nanoelectronics Research Institute, AIST Tsukuba Central 2, 1-1-1 Umezono, Tsukuba 305-8568, Japan ∗ E-mail: m-aoyagi@aist.go.jp, 2. Faculty of Science and Engineering, Waseda University 120-405 Smart Energy System Innovation Center, 513 Wasedatsurumaki, Shinjuku-ku 162-0041, Japan

Original manuscript received October 26, 2014, Revisions received July 29, 2015, Accepted July 30, 2015

the ordinary semiconductor IC.[3] The R&D for the SIP method has been conducted actively at a practical level for downsizing, speed increase, and low power consumption in mobile electronic devices, and the method has been incorporated into actual products. SIP is one of system integration technologies called “more than Moore” to achieve integration in the vertical direction that is on a different dimension from Moore’s Law that presents the proportional reduction of device size. It is thought to be complementary with the system integration method called the system on chip (SOC)[Term 2] where a certain size electronic system is embedded on an IC chip. However, the interconnections between the IC chips are done with relatively long wires including bonding wires and internal wiring in a package, and such structure is not suitable for high-speed or high-frequency operation. On the other hand, the 3D IC chip stacking technology, which is the technology to vertically stack multiple IC chips by forming micro-bump joints and through-Si-via (TSV)[Term 3] electrodes penetrate the substrate of the IC chip from surface to the back side, is highly expected as the technology that can achieve diverse high performances such as downsizing, high density, high speed, high performance, and low power consumption in electronic hardware.[4]-[6] It should be noted that the 3D IC chip stacking can respond to high-density integration of IC devices using different substrate materials and processes for which realization is difficult by SOC method. By extending the wiring space in the hardware from 2D to 3D, there is possibility for major changes in the configuration of the circuit and the system.

To realize a specific high-performance electronic device where the 3D IC chip stacking technology is applied at system level as a fundamental technology for high-density high-integration electronic hardware configuration, it is necessary to develop a prototyping technology of the 3D IC chip stacking system. By developing innovative circuit and system technology that thoroughly utilizes the merits of 3D IC chip stacking, it becomes possible to send out a next-generation hardware system integration technology into society.

Because the R&D items required for the realization of 3D IC chip stacking system spread across extremely diverse and multifarious technological fields, not all can be covered within the limited research resource at AIST. Therefore, we followed a scenario of engaging primarily in the technical issues in which the companies have fallen behind, yet are very important and very urgent, and we have engaged in the R&D for establishing fundamental technology for 15 years.

Figure 1 shows the progress so far of the electronic hardware system integration technology. First, the SOC technology that enables achievement of a high-performance system is a technology for integrating several circuit blocks that configure a certain size electronic system onto a large-scale IC chip. Compared to conventional large-scale IC development and manufacturing, the cost increases significantly due to the longer time required for SOC development and manufacturing. SOC commercial products will be hard to realize unless there is an IC chip that can be utilized in several commercial system products through a general-purpose circuit design and for which large-scale production over several million units is possible (such as in high-functional general-purpose CPUs[Term 4] and general-purpose image processors). Second, the SIP technology that allows compact integration of multiple IC chips is a technology to integrate multiple IC chips corresponding to the circuit block that configures the system into one package, and it is widely used as it allows significant reduction of development

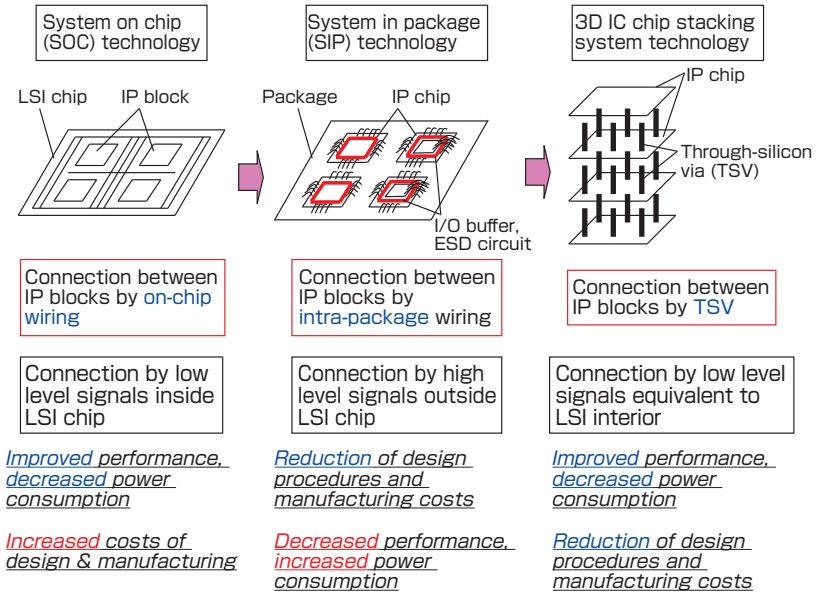

Fig. 1 Progress of electronic hardware system integration technology

and manufacturing costs in the consumer application fields that do not demand much high performance. Third, the 3D IC chip stacking technology, which uses TSVs and bump joints and is also called the ultimate SIP technology, is a technology that allows performance equivalent to SOC or even surpassing SOC by adopting a novel system architecture utilizing 3D wiring topology. There is a possibility for the significant reduction of its development and manufacture costs compared to SOC.[7] Against the sharp increase of cost for achieving nano-size device structure expected for next-generation nodes, improvement of the integration level while keeping down the total cost through 3D stacking is expected.

The merit for using the 3D IC chip stacking technology in digital systems is that increased system processing performance can be expected by employing the parallel processing architecture by multi-layering the functional circuit blocks such as the multi-core architecture.[8] To achieve this concept, the important key subject is to significantly raise the data communication capacity between the processing blocks. From this perspective, Fig. 2 shows the categorization of the IC chip stacking technology according to the signal transmission method between the chips embedded with processing IP[Term 5] blocks (called IP chips) that conducts various arithmetic logic processing. The chip stacking method by thin IC package stacking is appropriate for the construction of a general-purpose small system with emphasis on low cost. On the other hand, the chip stacking method by wireless connection using capacitive, inductive, or electromagnetic coupling is suitable for the construction of a robust system that requires high-speed transmission and high reliability due to avoiding physical connection. Also, the chip stacking method by a through Si via (TSV) that penetrates the substrate of the IC chip is suitable for the construction of high-performance low-cost systems using several TSVs. The chip stacking methods by optical waveguide connection using the optoelectronic packaging technology and silicon photonics[Term 6] technology are suitable for the construction of high end systems such as core networks and supercomputers that demand maximum level performance.

In this research, the final outcome is set as the preparation of the R&D environment for design, prototyping, and evaluation of the practical hardware system using the 3D IC chip stacking technology, that are necessary to widely diffuse into society, as well as the verification of typical prototype application system that takes advantage of the 3D IC chip stacking.

3 Manufacturing process for the 3D IC chip stacking and preparation of the total design environment

3.1 Elemental technologies for the manufacturing process of the 3D IC chip stacking

Since the corporate R&D engineers pay attention to the new method as a way to increase the degree of integration in semiconductor devices, engaging in the development of 3D IC chip stacking process at the wafer level, even in the R&D phase, would be the general approach, assuming the progression to the mass production process.[9]-[15] However, though it may seem to be a long route to take, AIST has engaged in the R&D aiming for the construction of a highly efficient rapid prototyping environment, and concentrating on the 3D IC chip stacking process at chip level that enables manufacturing at high yield and short production time using the low-cost process devices. Particularly, the 3D IC stacking and packaging process at chip level is highly compatible with the minimal fab[Term 7] concept proposed by AIST as a semiconductor device manufacturing system using small 0.5-inch size Si wafers, and we shall emphasize the possibility of constructing a minimal 3D stacking process line that

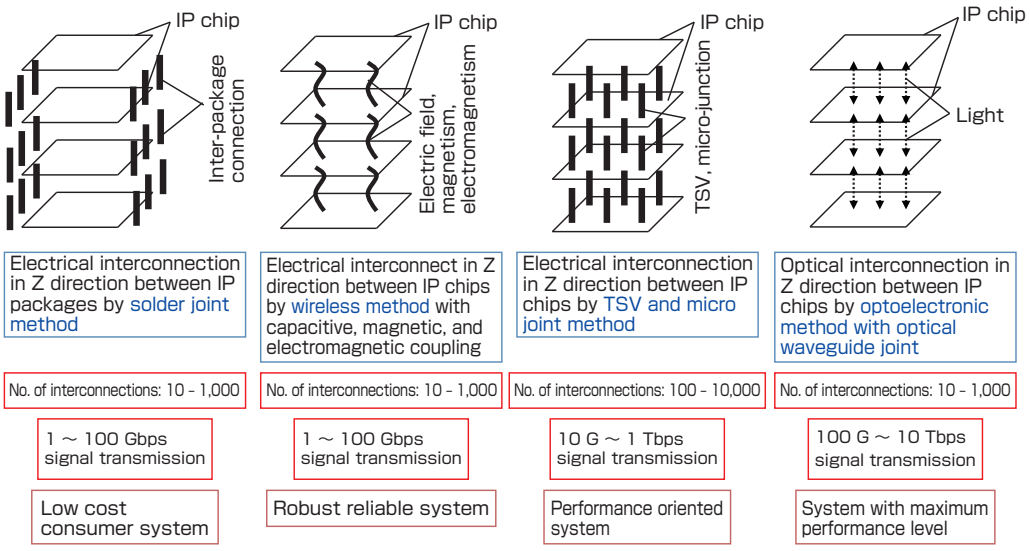

Fig. 2 3D IC chip stacking system technology

includes all manufacturing processes from semiconductor IC device manufacture to stacking and packaging.[16]

In the general 3D IC stacking manufacturing process, the process flow is as follows: the deep embedded through Si substrate via electrodes are formed from the surface toward the back side after a regular CMOS semiconductor manufacturing process, the silicon substrate is thinned from the back side to expose the bottom of the via hole electrodes, wiring is formed on the back side, the metal micro-bumps are formed on the wiring using soldering material, and the bump joints are formed between the stacked devices using high-precision bonding technology. In this manufacturing process flow, the process of forming the through-silicon-via (TSV) electrode that penetrates the silicon substrate is the core process from the points of difficulty and cost. Specifically, as shown in Fig. 3, it is a series of processes where the deep through via holes are etched by the Bosch method from the surface to the back side of the silicon substrate, the via holes are filled with metal by an electroplating process after forming barrier and insulating layers on the wall of the via holes by the CVD method, the electrodes are exposed on the surface by a smoothing technique such as the CMP method, and further thinning is done from the back side by grinding, CMP, and RIE methods to expose the electrodes at the bottom of the via holes to form completely penetrating electrodes.

Figure 4 lists the development items of the fundamental technologies (process and evaluation) of the 3D IC chip stacking system integration that were developed at AIST. The specific items include the following. Elemental technologies for chip stacking process are the following: low-volume, low-resistance, and low internal stress TSV structure using low-k organic insulator;[17] micro-pitch, high-density, and micro-bump connection formed by a thermo-compression method using cone-shaped micro-bumps;[18]-[20] electroless plating connection for power source pads where the power source pad electrodes

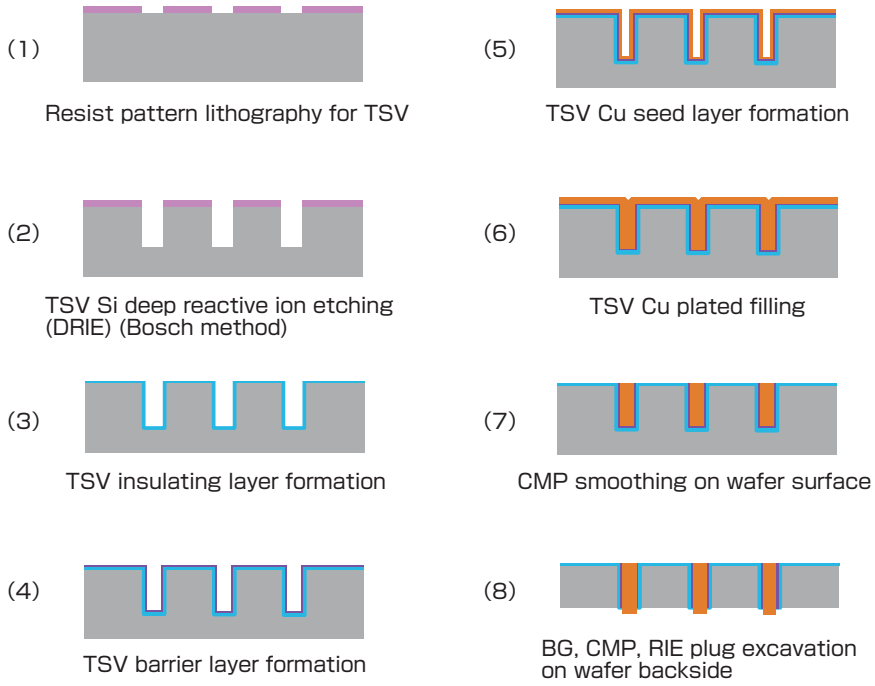

Fig. 3 Process flow for manufacturing the TSV

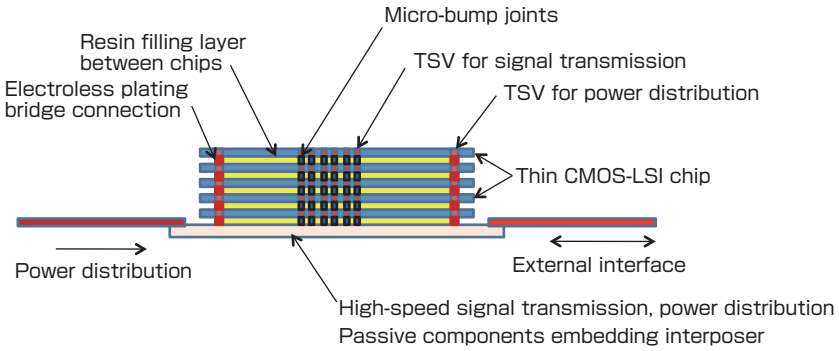

Fig. 4 Fundamental technologies for the 3D IC chip stacking system integration (stacking process and evaluation test)

are connected by direct Ni-B and Au electroless plating after chip stacking;[21][22] interposer with passive components where the thin film capacitors or the chip capacitors are embedded in the substrate;[23][24] and others. Evaluation and inspection technologies are as follows: evaluation of electrical property in local fine structures using high-speed sharp step signals with 10-ps rising time;[25] evaluation of 20 Gbps high-speed digital signal transmission;[26] evaluation of power supply wiring impedance using impedance analyzer for 10 Hz - 40 GHz super-wide bandwidth;[27] inspection of good chips where electrical testing can be done at chip level using the membrane fine pitch contact probe;[28] boundary scan embedded test circuit where total electrical connection test of fine interconnects can be conducted after stacking;[29] high-speed inspection of cone-shape micro-bumps where wafer level shape optical inspection can be conducted by laser illumination and high-speed high-resolution image sensors;[30] and others.

As an example of the development of a low-volume, low-resistance, and low internal stress TSV structure, we describe the development of a TSV structure using the parylene organic resin as the insulating layer of the TSV sidewall.[17] Figure 5 shows the manufacturing process flow of the TSV structure with parylene sidewall insulating layer, where the uniform parylene thin film was formed using low-temperature CVD method. Figure 6 shows the cross-sectional SEM photograph after the formation of a parylene sidewall insulating layer in the TSV manufacturing process. Compared to the sidewall insulating layer made of inorganic insulating materials such as SiO_2 or SiN_x, good coverage with uniform and thick parylene film can be achieved. Figure 7 shows the cross-sectional SEM photograph after parylene sidewall insulating layer formation and Cu plating in the TSV manufacturing process. The filling of TSV holes with Cu metal can be done by the Cu electroplating method. For suppressing the internal stress produced around the sidewall insulating layer due to the different thermal expansion coefficient of Cu and Si, the internal stress relaxation in the Si substrate can be achieved due to the elastic deformation of the parylene film.

Next, as an example of the development of fine-pitch high-density micro-bump interconnections, we describe cone-shaped micro-bump interconnections formed by the nanoparticle deposition (NPD) method.[19] Figure 8 shows the SEM observation photograph of the cone-shaped gold (Au)

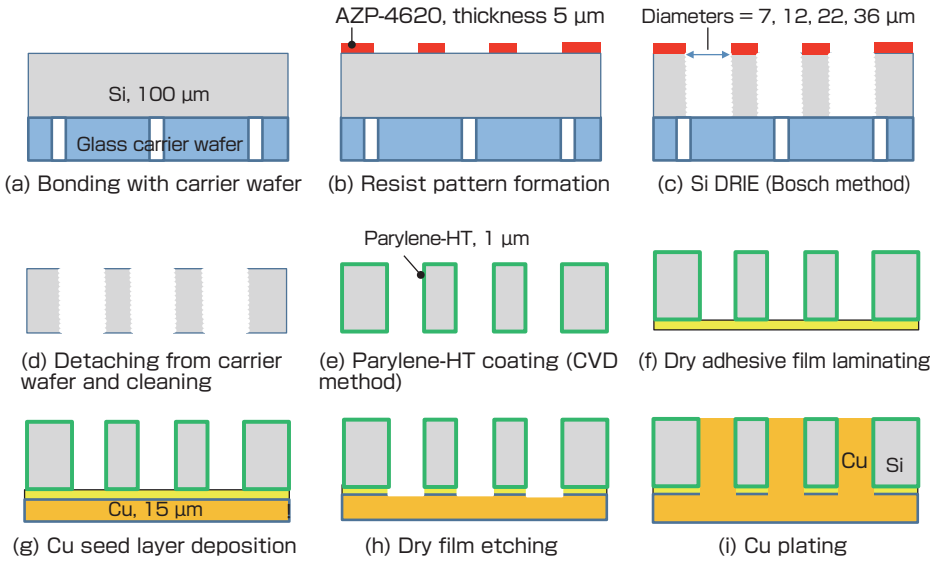

Fig. 5 Process flow for manufacturing the parylene sidewall insulating layer TSV structure

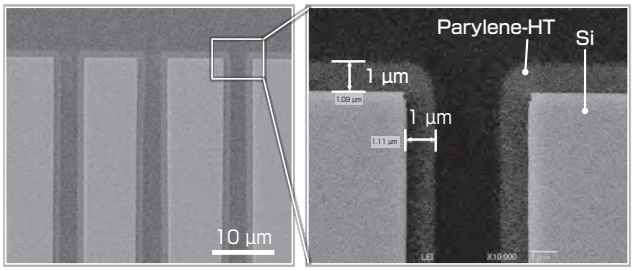

Fig. 6 Cross-sectional SEM photograph after the formation of parylene sidewall insulating layer in the TSV structure

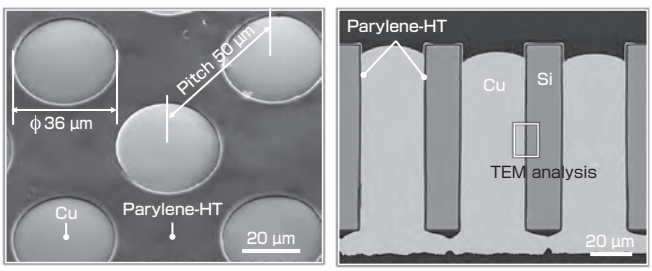

Fig. 7 Cross-sectional SEM photograph after Cu plating and filling of parylene sidewall insulating layer in the TSV structure

micro-bump array formed by the nanoparticle deposition method, where the Au nanoparticles are produced in the He gas atmosphere by an evaporating method, and the deposition is done by ejecting the He gas with the Au nanoparticles through a small bore nozzle. The cone-shaped micro-bumps have a diameter of 10 μm and a height of 12 μm, and are arranged in a 100 × 100 (10,000 bumps) array at a pitch of 20 μm. The cone-shaped Au bumps are formed with a self-assembly manner in a hole structure, as the film is formed as the substrate is scanned while the Au nanoparticles are sprayed from small bore nozzles, after the round hole photo resist mask is formed on the substrate, and at the same time, a peak structure grows at the upper end edge of the mask hole. Figure 9 shows the cross-sectional SEM photograph of one cone-shaped bump interconnection structure formed by the thermal compression method using a cone-shaped Au bump. By a thermo-compression process at temperature of 200 ºC, the bump height is compressed 44 % from 12.6 μm to 7.1 μm, and the 8.6 mΩ low-resistance connection can be achieved. The compression level can be controlled by the applied pressure.

By constructing the 3D IC chip stacking process environment at chip level, it is possible to meet the demand for rapid prototyping in the R&D phase. Also, through the construction

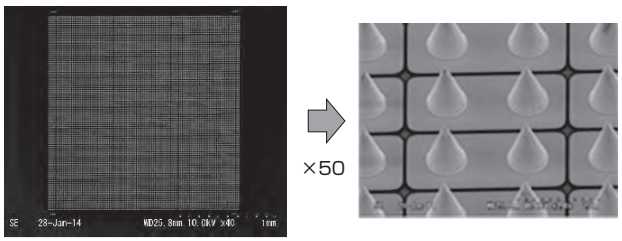

Fig. 8 SEM photograph of the 10,000 (100 x 100) cone-shaped Au micro-bump array (partially enlarged x50)
(Diameter: 10 μm, height: 12 μm, pitch: 20 μm)

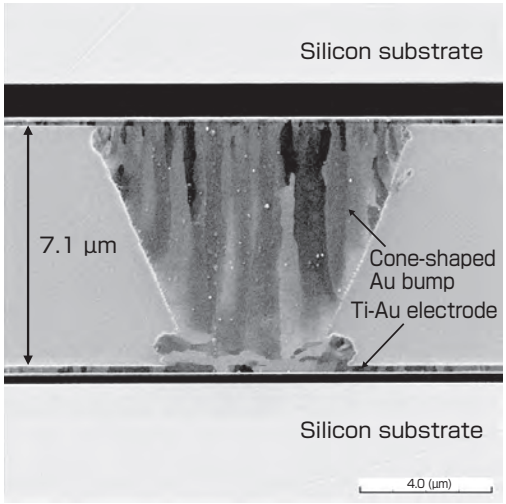

Fig. 9 Cross-sectional SEM photograph of the single cone-shaped bump connection structure

of the multi-physics design and analysis environment, we are organizing the integrated analysis environment for multiple CAD tools where the electric, thermal, and mechanical properties can be comprehensively designed and analyzed in an integrated manner, as well as a seamless design environment where the design data can be handed over efficiently from upstream to downstream, or from IC device design to total system design. This will enable total integrated design in the final practical phase.

From the above development scenario, by using the physical hardware integration environment for the 3D IC chip stacking, we believe we can contribute to creating circuit and architecture technology with a completely new concept that cannot be realized with the conventional 2D IC. Specifically, by utilizing over 1,000 multi-channel electric connections among the stacked devices, we aim to produce a new system function that utilizes the high-capacity interface communication among the stacks.

3.2 Integration method in the 3D IC chip stacking system

In the design phase of the 3D IC chip stacking system, it is necessary to design a large-scale integrated circuit based on the 3D IC stack standard cell library that is the basic unit of design containing fine components (TSV electrode, metal micro-bump interconnection, inter-stack resin interfill, heat dissipation layer, etc.) with greatly varying properties (electric, thermal, mechanical, etc.). Therefore, it is necessary to design and make a prototype for the evaluation TEG[Term 8] device in varying designs with different design parameters, for the standard cells used as basic component units needed for design. Then, by comprehensively conducting property evaluations for electric, thermal, and mechanical properties, the 3D IC stacking design tool kit is prepared including a design guideline and design rules, not just the layout design library of the standard cells. By preparing the design tool kits through a series of tasks for design, prototyping, and evaluation using TEG or prototype devices repeated several times, we aim to achieve the matured level that ultimately enables design, prototyping, and evaluation of the practical system.

As an example of development of the IC design technology that coordinates electrical and thermal properties, we describe the development of an IC design flow constructed by introducing an IC thermal analysis software, based on the existing IC design tool.[31] Figure 10 shows the process flow of the IC thermal analysis in the electrothermal IC design. First, the conventional logic IC design tool is used for logic design simulation and circuit placement and wiring, and valuation is done by calculating the values of the average power consumption at a standard cell unit that is the basic unit of IC design, and then by allotting the values of consumed power to all transistors arranged in the cell. Based

on the layout design data with allotted power consumption values, IC thermal analysis simulation is conducted using the transistor level thermal analysis software[32] that has been originally developed to enable efficient calculation. Figure 11 shows the flow of the thermally aware layout design data in electrothermal IC design using several design tools.

4 Verification R&D by design, prototyping, and evaluation using the TEG device for evaluation

The design and prototyping of evaluation TEG device will require funds in the hundred million yen range if conducted at wafer level, and this is not of the budget level of a research institute. On the other hand, using the shuttle service of the CMOS foundry where the design and prototyping of the CMOS semiconductor IC device at wafer level are conducted as shared multiple chip prototyping, the evaluation TEG device may be prototyped at one-tenth the required cost. We decided to conduct the R&D that assumes device prototyping using such a shuttle service.

For the IC device design, it is necessary to prepare a large-scale IC design CAD environment to conduct design independently, and that requires hundreds of millions of yen, and this cannot be undertaken easily by a laboratory. Authors Aoyagi and Nakagawa had used the CAD tool of Mentor Graphics Inc. 20 years ago to design the superconductor integrated circuit, but had to give up maintaining the tool environment since they were unable to pay the expensive licensing cost.

For the design, we decided to request cooperation of a fabless company that possessed a design environment and took design subcontracts. We searched for candidate companies,

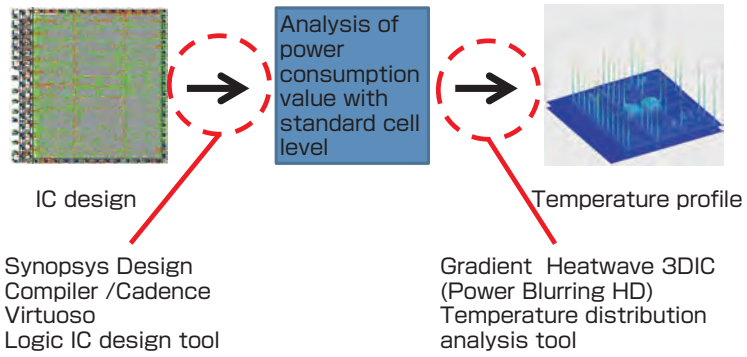

Fig. 10 Process flow for the IC thermal analysis in electrothermal IC design

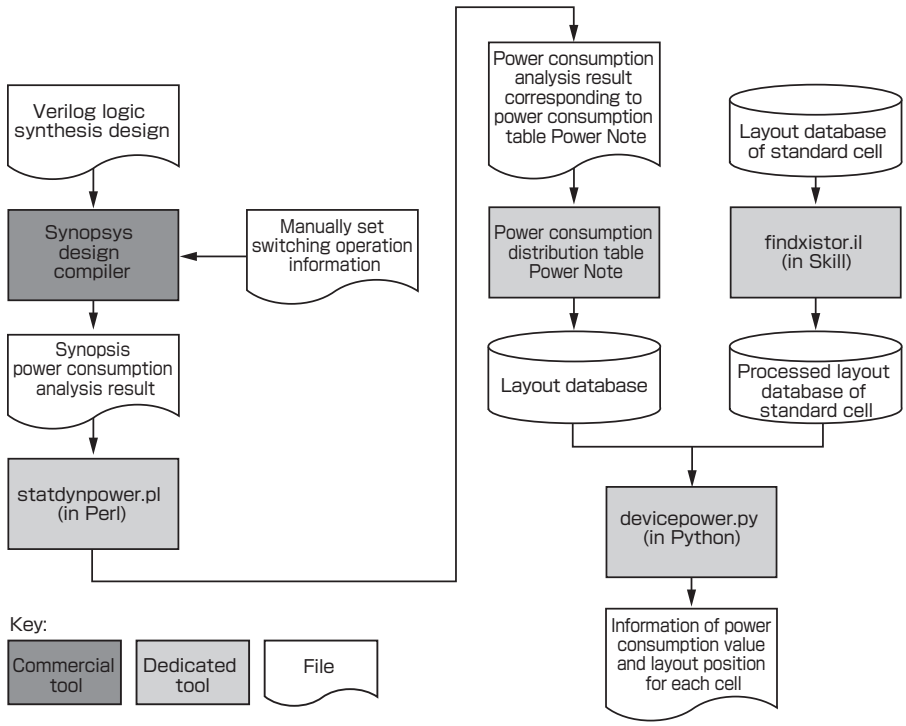

Fig. 11 Flow of design data for the thermal aware IC layout design regarding electrothermal IC design

and had a chance to meet Tops System Corporation that was established in our hometown Tsukuba in 1999.

In August 2007, the engineers of Tops System Corporation visited AIST to present the technologies for heterogeneous multi-core architecture TOPSTREAM that Tops System originally developed. We recognized the possibility that this may realize a new system design technology as the architecture was highly compatible with the 3D IC chip stacking system, and decided to collaborate.[33]

In 2008, the Supporting Grant for Small and Medium Enterprise from the Ministry of Economy, Trade and Industry was used to conduct the conceptual construction of the whole architecture including the IC stacking interface standard of Cool Interconnect, as the heterogeneous multi-core architecture for 3D IC chip stacking. Several patents were filed, and specific fundamental technology development was done for the stacking interface. For establishing the stacking interface, the IC device prototyping that required lots of resources was avoided, and the first priority was given to the construction of the communication protocol and testing technology for stacking interface where our developed technologies could be applied to file patents.[34] Figure 12 shows the concept of the Cool Interconnect. This is a wide bus bi-directional communication interface specification for stacked chips, where 1,600 10 μm diameter TSVs at 50 μm pitch were formed at the center of thin IC chips with 50 μm thickness, and eight layer chip stacking interconnected by micro-bumps is assured as maximum level.

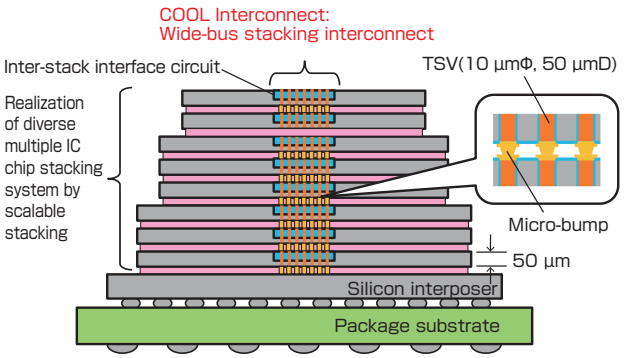

Fig. 12 Conceptual diagram of the Cool Interconnect

With the result of the conceptual investigation of the 3D IC stacking architecture including the stacking interface standard Cool Interconnect, we proposed a joint R&D project with Tops System Corporation for the R&D program of Innovative Energy-Saving Technology, New Energy and Industrial Technology Development Organization (NEDO) in May 2009. Fortunately, our proposal was selected, and through this NEDO R&D project, we were able to engage in the verification research of the 3D IC stacking architecture including the design and prototyping of the IC device. In this project, innovative energy-saving device technology that can achieve significant energy saving of the high-resolution image processing system through 3D IC stacking with heterogeneous multi-core architecture was developed. Figure 13 shows the concept on energy-saving in the 3D IC stacking system design using the Cool Interconnect.[35] This attempts to obtain sufficient power saving and high arithmetic logic operation performance by conducting efficient parallel processing using composite instructions, by reducing the clock frequency down to several 10 MHz and connecting the multiple diverse arithmetic logic processors through the Cool Interconnect.

We designed and prototyped the evaluation TEG consisting of a super-parallel bus interface circuit matching the 3D IC stacking, assuming the 1,600 TSVs and micro-bump interconnections based on the stacking interface standard Cool Interconnect. Then we evaluated the signal transmission property of 0.588 Gbps/1mW at low power consumption among the stacked devices connected face-to-face by micro-bumps. The stacking interface circuit was designed using the buffer and receiver circuits based on the

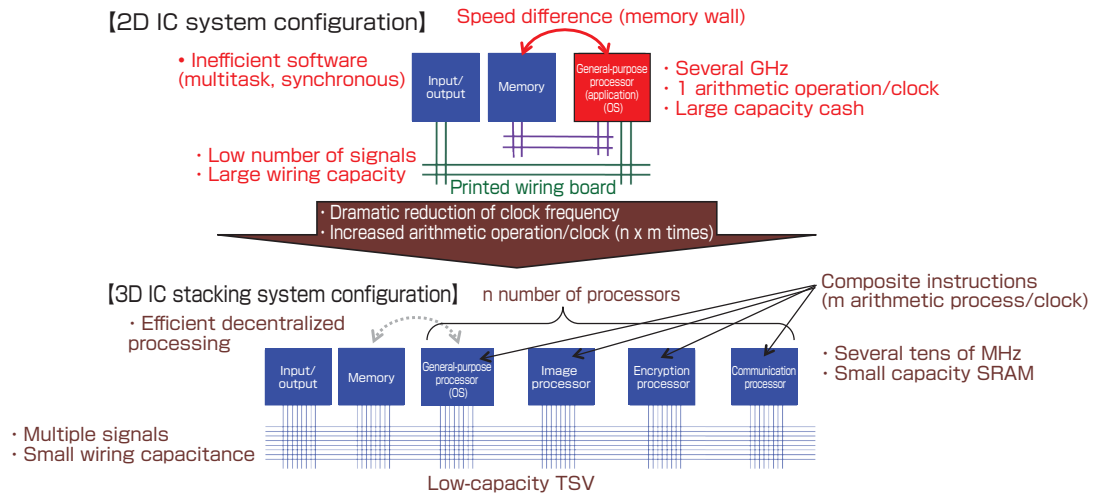

Fig. 13 Power saving in the 3D IC stacking system by Cool Interconnect

standard cells provided by CMOS device foundry, and high signal transmission capacity was realized by super-parallel interconnects without any special differential transmission circuits. For the formation of micro and low-capacitance TSV, in which the parasitic capacitance that affects the signal transmission property has been reduced, was designed and prototyped, and a low-capacitance property at 0.25 pF/TSV (2 pF even at eight stacks) was investigated for TSVs with a diameter of 10 µm and a depth of 50 µm by electrical evaluation. Unfortunately, the signal transmission property after stacking including the TSV could not be evaluated during the project period due to lack of research budget.

Figure 14 shows a photograph of the IC device for the Cool Interconnect functional evaluation test to investigate the signal transmission operation of the super-parallel bus interface circuit based on the Cool Interconnect specification. The TSVs and bumps for stacking interconnects were formed in the 2.16 mm square area in the center. The TSVs and bumps for GND and power sources: Vdd (2.5 V) and Vio (3.3 V) were formed around the four sides. The prototyping of the test IC device was done using the shuttle service of a 0.25 µm node CMOS foundry. Figure 15 shows the microphotograph observing the cross-sectional structure after face-to-face stacking by thermo- compression method using the test IC device on which the cone-shaped bumps (no TSV) were formed. Figure 16 shows the test IC device after stacking placed on the evaluation board. Figure 17 is the result of the evaluation experiment for the super-parallel bus interface transmission function incorporated in the device. It shows the power consumption in the interface circuits when the clock frequency was varied in the range of 2-50 MHz. Large signal transmission performance of 51.2 Gbps (1024 bit • 50 MHz) was demonstrated under a low power consumption condition of 87 mW.[36][37] For the interface circuit composed of a 0.25 µm node CMOS device that operates at power voltage of 2.5 V, large capacity transmission was achieved at sufficiently low power consumption. Further power saving can be expected by using a finer node CMOS device.

Based on the electrothermal IC design flow explained in Fig. 10, Fig. 18 shows the thermal analysis result of the temperature increase profile for the central part in the single Si chip placed on the ideal heat sink for the super-parallel bus interface communication interface circuit at 500 MHz operation (high clock frequency was set to emphasize heat generation).[19] The heat dissipation by heat sink is effective and the temperature increase is small. In the practical simulation analysis comparing the actual temperature measurement, the investigation for the thermal properties for the heat dissipation path will become important.

For the operability verification experiment after stacking using evaluation TEG including TSV, the prototype verification could not be done due to lack of development resources and development period, and the verification

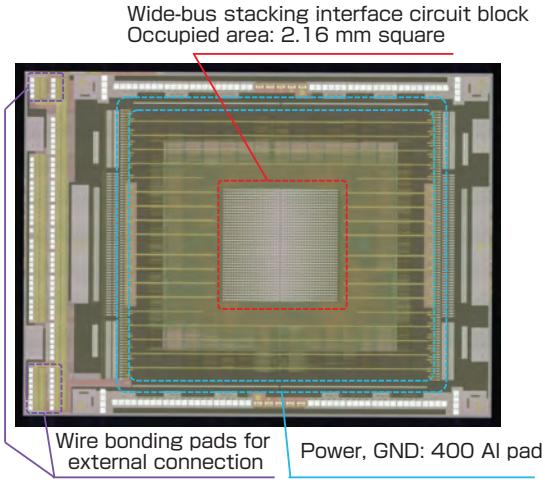

Fig. 14 Test IC device for Cool Interconnect evaluation

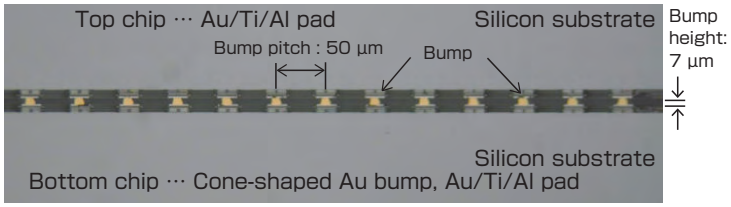

Fig. 15 Cross sectional microphotograph of bump connection structures after stacking by thermo-compression method

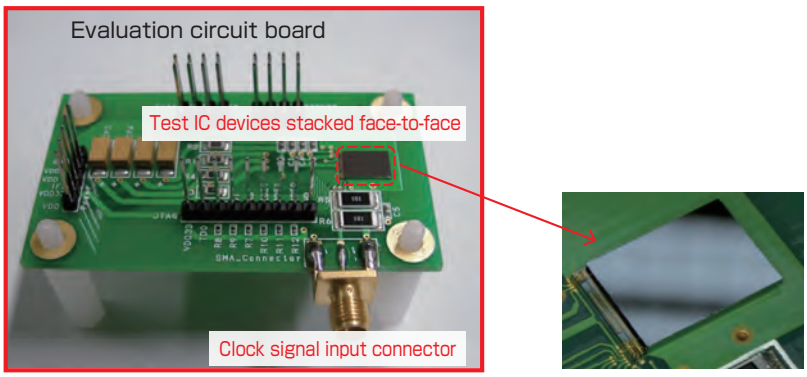

Fig. 16 Test IC device mounted on the evaluation circuit board after stacking

using more practical prototypes in the future R&D project is awaited.

5 Future prospect for the research results

The practical development of the 3D IC chip technology entered a new phase with the start of the NEDO project with its research base at AIST. Specifically, the NEDO Smart Device R&D Project[38] including the 3D various IC stacking technology that aims for real-time high-speed image processing by stacking the sensor device and signal processing device started in FY 2013, and the R&D is currently in progress. This R&D project includes the research plan for designing and prototyping the practical level CMOS-IC device at wafer level, with the participation of a design team of the manufacturer of the application system. At the same time, by the end of the project, we aim to become an open R&D center for 3D IC chip stacking prototyping in Japan by organizing the prototype production process line in AIST, where the 3D IC chip stacking process can be done at wafer level through the participation of the manufacturing device companies. The stacking process will be conducted at chip level for now, but the stacking process at wafer level will be studied concurrently with problem abstraction.

Table 1. History of the verification R&D

	Development history
2007	Consideration about combination of heterogeneous multi-core architecture and 3D IC chip stacking
2008	Basic research for stacked interface standard (Support Grant for Small and Medium Enterprise, METI)
2009-12	Verification research for stacked interface circuit (Innovative Energy Saving Project, NEDO)
2013-18	Currently engaging in practical development of 3D IC chip stacking technology (Next-Generation Smart Device Development Project, NEDO)

Lastly, the history of the verification R&D is summarized in Table 1.

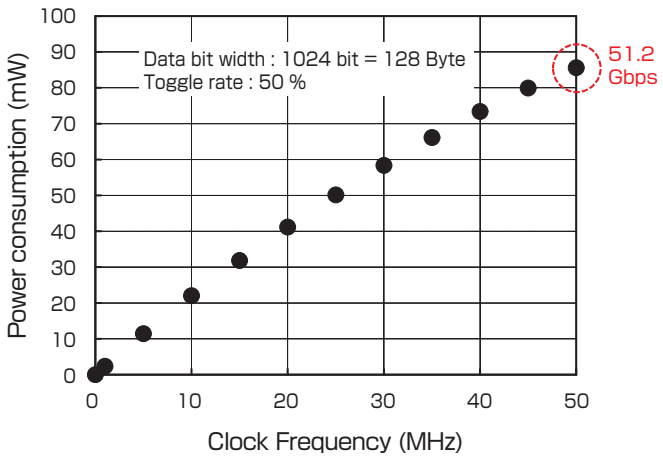

Fig. 17 Dependency of the power consumption on clock frequency in the parallel bus interface circuit

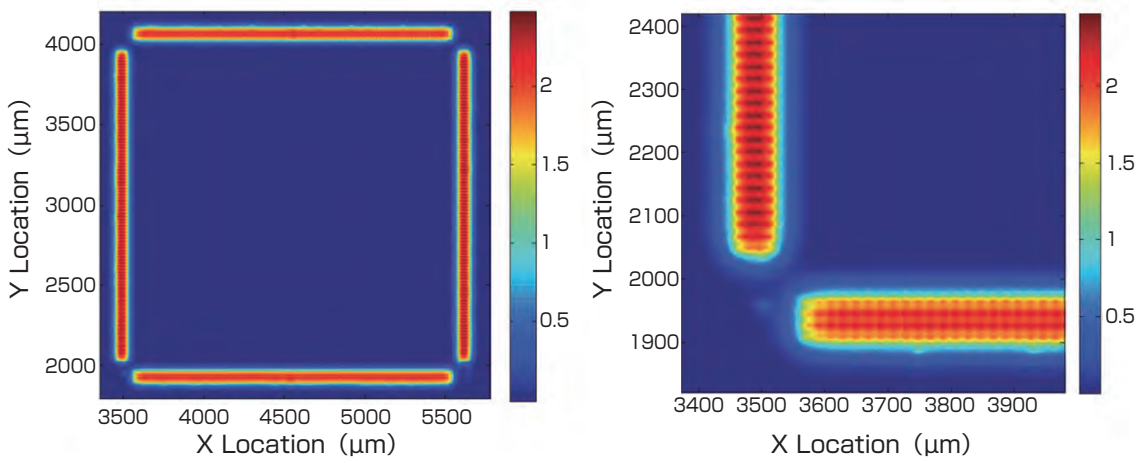

Fig. 18 Result of the simulation analysis for temperature profile in stacked interface circuits during 500 MHz operation

6 Future issues

It is necessary to pour enormous amount of human and research resources to construct the R&D environment for design, prototyping, and evaluation for a practical system that is the final outcome of this research. In order to integrate the fundamental technologies for which the R&D has been conducted and to advance further, we must spend effort to obtain considerable scale of research resources.

Various next-generation low power consumption device technologies are being developed. By combining such technologies and the 3D IC chip stacking technology, an innovative high-performance low power consumption system can be expected. Therefore, it is necessary to accelerate the development of innovative and high-performance circuit and system technologies that maximize the merit of 3D IC chip stacking, through cooperation of researchers and engineers in electronic circuit and system technology fields, and by utilizing the environment for design, prototyping, and evaluation of the 3D IC chip stacking system that matches the practical system. In the near future, we hope that the 3D IC chip stacking prototyping facility that will be constructed at AIST will be utilized effectively as the open innovation hub of industry-academia-government collaboration.

Terminologies

Term 1. System in package (SIP): The method for integrating multiple integrated circuit (IC) chips possessing functional operation into one package; by this method, we can build an IC system. In many configurations, various control circuit chips and memory chips are stacked around the central microprocessor chip on the package substrate.

Term 2. System on chip (SOC): The method for integrating multiple circuit blocks possessing functional operation onto one IC chip; by this method, we can build an IC system. In many chip configurations, various control circuits and memory circuits are integrated around the microprocessor core. Since ordinary IC chips are supplied according to each function, it is necessary to realize packaging and interconnecting for multiple chips on a package circuit substrate. However, in SOC, the system functions that are divided over several chips can be integrated in a single chip and supplied as a single chip.

Term 3. Through-silicon-via (TSV): The electrode that penetrates the substrate of a silicon IC chip in a vertical direction. It is used in the 3D IC chip stacking technology where multiple IC chips are stacked and integrated at high density.

Term 4. Central processing unit (CPU): The integrated circuit that functions as the major information processing device in a computer. It can execute various arithmetic logic processing, information processing, device control, etc. according to the program.

Term 5. Intellectual property (core) [IP (core)]: Partial circuit information to configure a part of an IC device, particularly the one bundled as a functional block. It may be simply called IP.

Term 6. Silicon photonics: The technology where fine optical waveguide structures are created on a silicon substrate that is widely used as an IC device, and the devices with various functions are integrated onto one small chip. Since this enables the integration combining IC devices and optical devices, it is gaining attention as a technology that may enable super-downsizing and power saving of the electronic system.

Term 7. Minimal fab: The innovative semiconductor manufacturing system proposed by AIST using a 0.5-inch wafer as the manufacturing substrate unit. The three features are as follow: (1) 0.5-inch diameter wafer, (2) manufacturing equipment size of 30-cm width, and (3) no clean room through a localized clean production system.

Term 8. Test element group (TEG): The IC chip for evaluation that is specially designed and manufactured to extract various design parameters, prior to the design and manufacture of the actual integrated circuit.

References

[1] Yano Research Institute Ltd.: *Keitai Denwa No Sekai Shijo Ni Kansuru Chosa Kekka 2015* (Survey of the World Market for Mobile Phones 2015), (2015) (in Japanese).

[2] J. Takei: CPU architecture no hensen (Transition of CPU architecture), Presentation material for the 8th Cyber Kansai Project Workshop (2012) (in Japanese).

[3] Japan Institute of Electronics Packaging: Technology roadmap on system in package, [Special Articles] Electronics packaging technology: The current status and perspective, *Journal of Japan Institute of Electronics Packaging*, 9 (1), 13-19 (2006) (in Japanese).

[4] M. Koyanagi, H. Kurino, K. W. Lee, K. Sakuma, N. Miyakawa and H. Itani: Future system-on-silicon LSI chips, *IEEE Micro*, 18 (4), 17-22 (1998).

[5] T. Fukushima, H. Kikuchi, Y. Yamada, T. Konno, J. Liang, K. Sasaki, K. Inamura, T. Tanaka and M. Koyanagi: New three-dimensional integration technology based on reconfigured wafer-on-wafer bonding technique, *IEEE Int. El. Devices Meet. (IEDM)*, 985-988 (2007).

[6] K. Takahashi, H. Terao, Y. Tomita, Y. Yamaji, M. Hoshino, T. Sato, T. Morifuji, M. Sunohara and M. Bonkohara: Current status of research and development for three-dimensional chip stack technology, *Jpn. J. Appl. Phys.*, 40, 3032-3037 (2001).

[7] J. M. Yannou: Roadmap Analysis: 3D Wafer Level Packaging, *ESTC2010 Workshop 3D WLP* (2010).

[8] IBM, Sony, SCEI and Toshiba: Press Release – Jisedai

Processor “Cell” No Shiyo Wo Kokai (IBM, Sony, SCEI and Toshiba released the technical specs for next-generation processor “Cell”) (2005) (in Japanese).

[9] M. Kawano, N. Takahashi, Y. Kurita, K. Soejima, M. Komuro and S. Matsui: Three-dimensional packaging technology for stacked DRAM with 3-Gb/s data transfer, *IEEE Trans. Electron Devices*, 55 (7), 1614 - 1620 (2008).

[10] T. Maebashi, N. Nakamura, Y. Sacho, S. Nakayama, E. Hashimoto, S. Toyoda and N. Miyakawa: High density assembly technology using stacking method, *IEEE 9th VLSI Packaging Workshop of Japan*, 149-152 (2008).

[11] P. Ramm, M. J. Wolf, A. Klumpp, R. Wieland, B. Wunderle, B. Michel and H. Reichl: Through silicon via technology - Processes and reliability for wafer-level 3D system integration, *Proc. 58th ECTC*, 841-846 (2008).

[12] J. U. Knickerbocker, P. S. Andry, B. Dang, R. R. Horton, C. S. Patel, R. J. Polastre, K. Sakuma, E. S. Sprogis, C. K. Tsang, B. C. Webb and S. L. Wright: 3D silicon integration, *Proc. 58th ECTC*, 538-543 (2008).

[13] M. Motoyoshi: Through-silicon via (TSV), *Proc. IEEE*, 97 (1), 43-48 (2009).

[14] U. Kang, HJ. Chung, S. Heo, SH. Ahn, H. Lee, SH. Cha, J. Ahn, DM. Kwon, J. H. Kim, JW. Lee, HS. Joo, WS. Kim, HK. Kim, EM. Lee, SR. Kim, KH. Ma, DH. Jang, NS. Kim, MS. Choi, SJ. Oh, JB. Lee, TK. Jung, JH. Yoo and C. Kim: 8 Gb 3D DDR3 DRAM using through-silicon-via technology, *ISSCC Digest of Technical Papers*, 130-131 (2009).

[15] M. Scannell, G. Poupon, L. Di Cioccio, D. Henry, J. C. Souriau, F. Grossi, P. Leduc, P. Batude, M. Vinet, P. Geugen, L. Clavelier and N. Sillon: 3D packaging and interconnect technologies at CEA-Leti Minatec, *Proc. ICEP*, 191-195 (2009).

[16] *Minimal Fab Handbook*, Sangyo Times (2013) (in Japanese).

[17] B.T. Tung, X. Cheng, N. Watanabe, F. Kato, K. Kikuchi and M. Aoyagi: Investigation of low-temperature deposition high-uniformity coverage parylene-HT as a dielectric layer for 3D interconnection, *Proc. 64th ECTC*, 1926-1931 (2014).

[18] Y. Gomi, Y. Hosaka, H. Hirabayashi, Y. Wakabayashi, H. Yamagishi, H. Ohsato, Y. Yamaji, K. Kikuchi, Y. Okada, H. Nakagawa and M. Aoyagi: Formation of pyramid-shape Au micro-bumps for high-density LSI packaging, *Proceedings of the 16th Microelectronics Symposium*, 23-26 (2006) (in Japanese).

[19] F. Imura, X. J. Liu, S. Nemoto, F. Kato, K. Kikuchi, M. Suzuki, H. Nakagawa, M. Aoyagi, Y. Gomi, I. Saito and H. Hasegawa: Au cone-bump by nanoparticle deposition technology, *Proceedings of the 25th JIEP Anuual Meeting*, 229-232 (2011) (in Japanese).

[20] F. Imura, N. Watanabe, S. Nemoto, W. Feng, K. Kikuchi, H. Nakagawa and M. Aoyagi: Development of micro bump joints fabrication process using cone shape Au bumps for 3D LSI chip stacking, *Proc. 64th ECTC*, 1915-1920 (2014).

[21] Y. Yamaji, T. Yokoshima, N. Igawa, K. Kikuchi, H. Nakagawa and M. Aoyagi: A method of fabricating bump-less interconnects applicable to wafer-scale flip-chip bonding, *Proc. 10th EPTC*, 657-662 (2008).

[22] T. Yokoshima, Y. Yamaji, K. Kikuchi, H. Nakagawa and M. Aoyagi: A method of “chemical flip-chip bonding” without loading and heating for ultra-fine chip-to-substrate interconnects, *Proc. 59th ECTC*, 80-86 (2009).

[23] K. Kikuchi, K. Takemura, C. Ueda, O. Shimada, T. Gomyo, Y. Takeuchi, T. Okubo, K. Baba, M. Aoyagi, T. Sudo and K. Otsuka: Low-impedance power distribution network of decoupling capacitor embedded interposers for 3-D integrated LSI system, *Proc. 18th EPEPS*, 25-28 (2009).

[24] K. Kikuchi, M. Aoyagi, M. Ujiie and S. Takayama: Development of decoupling capacitor embedded interposers using narrow gap chip parts mounting technology with wideband ultralow PDN impedance, *Proc. EDAPS*, 9-12 (2013).

[25] M. Aoyagi, K. Kikuchi, M. Suzuki and H. Nakagawa: High resolution electrical measurement technology for fine structures in 3D LSI chip stacking integration technology, *IEICE Transactions on Electronics Japanese Edition*, J93-C (11), 388-398 (2010) (in Japanese).

[26] K. Kikuchi, H. Oosato, S. Itoh, S. Segawa, H. Nakagawa, K. Tokoro and M. Aoyagi: 10-Gbps signal propagation of high-density wiring interposer using photosensitive polyimide for 3D packaging, *Proc. 56th ECTC*, 2, 1294-1299 (2006).

[27] K. Kikuchi, C. Ueda, K. Takemura, O. Shimada, T. Gomyo, Y. Takeuchi, T. Ookubo, K. Baba, M. Aoyagi, T. Sudo and K. Otsuka: Low-impedance evaluation of power distribution network for decoupling capacitor embedded interposers of 3D integrated LSI system, *Proc. 60th ECTC*, 1455-1460 (2010).

[28] N. Watanabe, M. Eto, K. Kawano and M. Aoyagi: Fine-pitch probing on TSVs and microbumps using a chip prober having a transparent membrane probe card, *Proc. 64th ECTC*, 2003- 2007 (2014).

[29] M. Aoyagi, F. Imura, S. Melamed, S. Nemoto, N. Watanabe, K. Kikuchi, H. Nakagawa, M. Hagimoto and Y. Matsumoto: Development of testing technology for wide bus chip-to-chip interconnection in 3D LSI chip stacking system, *Workshop Digest of 4th IEEE International Workshop on Testing 3D Stacked ICs* (2013).

[30] M. Aoyagi, N. Watanabe, M. Suzuki, K. Kikuchi, S. Nemoto, N. Arima, M. Ishizuka, K. Suzuki and T. Shiomi: New optical three dimensional structure measurement method of cone shape micro bumps used for 3D LSI chip stacking, *Proc. 3DIC*, 1-5 (2013).

[31] S. Melamed, F. Imura, M. Aoyagi, H. Nakagawa, K. Kikuchi, M. Hagimoto and Y. Matsumoto: Method for back-annotating per-transistor power values onto 3DIC layouts to enable detailed thermal analysis, *Proc. ICEP 2014*, 239-242 (2014).

[32] S. Melamed, T. Thorolfsson, T. R. Harris, S. Priyadarshi, P. Franzon, M. B. Steer and W. R. Davis: Junction-level thermal analysis of 3D integrated circuits using high definition power blurring, *IEEE Trans. Comput.-aided Design Integr. Circuits Syst.*, 31 (5), 676-689 (2012).

[33] Y. Matsumoto and T. Nakamura: Scalable multi-core SoC platform for low-powered architecture, *Proc. Cool Chips X*, (2007).

[34] M. Chacin, H. Uchida, M. Hagimoto, T. Miyazaki, T. Ohkawa, R. Ikeno, Y. Matsumoto, F. Imura, M. Suzuki, K. Kikuchi, H. Nakagawa and M. Aoyagi: COOL interconnect low power interconnection technology for scalable 3D LSI design, *Proc. Cool Chips XIV*, 1-3 (2011).

[35] Y. Matsumoto, T. Morimoto, M. Hagimoto, H. Uchida, N. Hikichi, F. Imura, H. Nakagawa and M. Aoyagi: Cool System scalable 3D stacked heterogeneous Multi-Core/ Multi-Chip architecture for ultra low-power digital TV applications, *Proc. Cool Chips XV*, 1-3 (2012).

[36] F. Imura, S. Nemoto, N. Watanabe, F. Kato, K. Kikuchi, H. Nakagawa, M. Hagimoto, H. Uchida, T. Omori, Y. Hibi, Y. Matsumoto and M. Aoyagi: 3D interconnect technology by the ultrawide-interchip-bus system for 3D stacked LSI systems, *IEICE Technical Report*, 112 (170), 43-48 (2012) (in Japanese).

[37] M. Aoyagi, F. Imura, S. Nemoto, N. Watanabe, F. Kato,

K. Kikuchi, H. Nakagawa, M. Hagimoto, H. Uchida and Y. Matsumoto: Wide bus chip-to-chip interconnection technology using fine pitch bump joint array for 3D LSI chip stacking, *Proc. IEEE CPMT Symposium Japan (ICSJ)*, 183-186 (2012).

[38] NEDO Next Generation Smart Device Development Project, http://www.nedo.go.jp/activities/ZZJP_100059.html, accessed 2013-10-31 (in Japanese).

Authors

Masahiro AOYAGI

Graduated from the Department of Electronic Engineering, Faculty of Engineering, Nagoya Institute of Technology in 1982. Joined the Electrotechnical Laboratory, Agency of Industrial Science and Technology, Ministry of International Trade and Industry in 1982. Engaged in the R&D of integrated circuit and system for superconductor device, high-speed high-density packaging system technology, and others. Obtained doctorate (Engineering) from the Nagoya Institute of Technology in 1991. Visiting Researcher, National Physical Laboratory, UK during 1994-1995. Group Leader, High-Density SI Group, Nanoelectronics Research Institute, AIST in 2001; Group Leader, 3D Integration System Group, Nanoelectronics Research Institute, AIST in 2011; and Deputy Director, Nanoelectronics Research Institute, AIST in 2012. Unit Leader, Collaboration Promotion Unit, Tsukuba Innovation Arena Central Office, AIST in 2015. Collaborative Professor, Saitama University. Member of the Japan Institute of Electronics Packaging, Japan Society of Applied Physics, Institute of Electrical Engineers of Japan, Japan Society of Mechanical Engineers, Surface Finishing Society of Japan, IEEE, IMAPS, IET, SPIE, and ASME. In charge of the R&D for overall 3D packaging technology.

Fumito IMURA

Graduated from the Department of Electric System Engineering, Faculty of Engineering, Kumamoto University in 2002. Completed the doctor's course at the Department of System Informatics, Graduate School of Science and Technology, Kumamoto University in 2007. Doctor (Engineering). Joined the Nanoelectronics Research Institute, AIST in 2007 as post-doctoral fellow. Researcher, Minimal Fab Development Association in 2012. Supporting Researcher, Nanoelectronics Research Institute, AIST in 2015. In charge of the R&D for fundamental technology in 3D stacking and packaging.

Fumiki KATO

Graduated from the Ritsumeikan University in 2004. Completed the doctor's course at the Department of Frontier Science and Technology, Graduate School of Science and Engineering, Ritsumeikan University in 2009. Doctor (Engineering). Joined the Nanoelectronics Research Institute, AIST in 2009 as post-doctoral fellow. Post-doctoral Fellow, Advanced Power Electronics Research Center, AIST in 2012. Limited-term Researcher, Advanced Power Electronics Research Center, AIST in 2014. Member of the Japan Institute of Electronics Packaging. In charge of the R&D for heat dissipation technology in 3D stacking and packaging.

Katsuya KIKUCHI

Graduated from the Department of Electric and Electronic Engineering, Faculty of Science and Engineering, Saitama University in 1996. Completed the doctor's course at the Department of Mathematics, Electronics and Informatics, Graduate School of Science and Engineering, Saitama University in 2001. Doctor (Engineering). Joined the High-Density SI Group, Nanoelectronics Research Institute, AIST in 2001. Has engaged in the R&Ds for next-generation electronic packaging technology centering on 3D packaging in LSI electronic packaging technology, ultra-high-speed high-frequency packaging technology, and measurement and evaluation technology. Joined the 3D Integration System Group, Nanoelectronics Research Institute, AIST in 2011; and Group Leader in 2015. Member of the IEICE, Japan Institute of Electronics Packaging, Japan Society of Applied Physics, and IEEE. In charge of the R&D for evaluation technology of 3D stacking and packaging design.

Naoya WATANABE

Completed the doctor's program at the Graduate School of Computer Science and Systems Engineering, Kyushu Institute of Technology in 2004. Doctor (Informatics). Joined the Kyushu Institute of Technology, Kumamoto Techno Industry Foundation, and Fukuoka Industry, Science and Technology Foundation. Became Researcher, Nanoelectronics Research Institute, AIST in 2011. Member of the IEEE, Japan Institute of Electronics Packaging, and Japan Society of Applied Physics. In charge of the R&D for fundamental technology of 3D stacking and packaging.

Motohiro SUZUKI

Graduated from the Department of Electronic Engineering, Graduate School of Engineering, Nagoya Institute of Technology in 1983. Joined the Electrotechnical Laboratory, Agency of Industrial Science and Technology, Ministry of International Trade and Industry in 1983. Joined the High-Density SI Group, Nanoelectronics Research Institute, AIST in 2007; Research Evaluation Promotion Office, Evaluation Department, AIST in 2009; High-Density SI Group in 2010; 3D Integration System Group in 2011; and retired in 2013. Member of the Japan Institute of Electronics Packaging, Japan Society of Applied Physics, and Information Processing Society of Japan. In charge of the R&D for electric evaluation technology in 3D packaging.

Hiroshi NAKAGAWA

Graduated from the Tokyo University of Science in 1978, and obtained doctorate (Engineering) at the Tokyo University

of Science in 1996. Joined AIST and engaged in researches for superconducting IC, high-density electronic packaging technology, and power electronics packaging technology. Member of the Japan Institute of Electronics Packaging, Institute of Electrical Engineers of Japan, and Japan Society of Applied Physics. In charge of the R&D for fundamental 3D packaging technology.

Yoshikuni OKADA

Graduated from the Department of Electronic Engineering, Graduate School of Engineering, Nagoya Institute of Technology in 1965. Completed the doctor's course at the Graduate School of Engineering, Nagoya Institute of Technology in 1970. Joined the Electrotechnical Laboratory, Agency of Industrial Science and Technology, Ministry of International Trade and Industry in 1970. Worked at the Logic System, Distributing System, Information Base Laboratory, and as Director, Computing Center. Joined the New Information Processing Research, Real World Computing Project in 1999; and Knowledge Intelligence Laboratory Co., Ltd. in 2002. Joined the High-Density SI Group, Nanoelectronics Research Institute, AIST in 2004; and retired in 2010. Member of the Information Processing Society of Japan. In charge of the R&D for 3D packaging interface technology.

Tokihiko YOKOSHIMA

Graduated from the Department of Applied Chemistry, Faculty of Science and Engineering, Waseda University in 1997. Completed the doctor's course at the Waseda University in 2002. Doctor (Engineering). Assistant, Faculty of Science and Engineering, Waseda University in 2001; Visiting Lecturer, Waseda Research Institute for Science and Engineering; and Visiting Lecturer, Kagami Memorial Research Institute for Materials Science and Technology, Waseda University (dispatched to Akita Research Institute of Advanced Technology) in 2004. Research Fellow, Electronics Research Institute, AIST in 2005. In charge of the R&D for 3D packaging process technology. Currently, Senior Researcher and Professor, Faculty of Science and Engineering, Waseda University.

Yasuhiro YAMAJI

Graduated from the Department of Metallurgy, Graduate School of Science and Engineering, Tokyo Institute of Technology in 1983. Completed the master's course at the Department of Material Sciences, Interdisciplinary Graduate School of Science and Engineering, Tokyo Institute of Technology in 1985. Joined the Toshiba Corporation in 1985. Was in charge of advanced LSI package development at the Semiconductor Business Division. Dispatched to the Association of Super-Advanced Electronics Technologies in 1999. Technical Staff, Nanoelectronics Research Institute, AIST in 2007. Completed the doctor's program at the Saitama University Graduate School in 2010. Doctor (Engineering). In charge of the R&D for 3D packaging process technology. Currently, working at the Development Division of J-Devices Corporation.

Shunsuke NEMOTO

Completed the master's program at the Iwaki Meisei University in 2006. Joined the Alps Business Service Co., Ltd. in 2006. Technical Staff, Nanoelectronics Research Institute, AIST in 2009. Enrolled in the doctor's program at the Saitama University Graduate School in 2015. Member of the IEICE and Japan Institute of Electronics Packaging. In charge of the R&D for 3D packaging process technology.

Tung Thanh BUI

Graduated from the Vietnam National University in 2004. Researcher, MEMS and Microsystems Laboratory, Electronics and Electrical Engineering Department, Vietnam National University in 2006. Completed the master's program at the Department of Creative Science and Engineering, Graduate School of Science and Engineering, Ritsumeikan University in 2008. Completed the doctor's program at the Department of General Science and Engineering, Graduate School of Science and Engineering, Ritsumeikan University in 2011. Doctor (Engineering). Research Fellow, Nanoelectronics Research Institute, AIST in 2011. In charge of the R&D for opto-electronics packaging technology and 3D packaging process technology.

Samson MELAMED

Graduated from the Department of Computer Sciences, University of Maryland in 2004. Completed the master's program at the Department of Electrical Engineering, University of North Carolina in 2007. Completed the doctor's program at the Department of Electrical Engineering, University of North Carolina in 2011. PhD. JSPS Research Fellow (short-term), AIST in 2012; Postdoctoral Fellow, AIST in 2013; and JSPS Research Fellow (long-term) in 2014. In charge of the R&D for 3D packaging design analysis technology.

Discussions with Reviewers

1 Positioning of this paper

Comment (Naoto Kobayashi, Center for Research Strategy, Waseda University)

This paper describes the scenario for the development of 3D IC chip stacking technology, explains the fundamental technologies to realize the goals of the scenario, as well as discusses the integrated design technology and the results. I think the paper is appropriate for *Synthesiology*. However, the most important research goal, its characteristic, and the details of the intermediate integrating technology that combines the fundamental technologies are still unclear. Therefore, I think you should elaborate on those points, and add some descriptions and

diagrams that overview the whole research.

Answer (Masahiro Aoyagi)

I think we have not reached the research phase where we can clearly describe the "intermediate integrating technology that combines the fundamental technologies." If we are given an opportunity to write a follow-up report, we will be delighted to take on the interdisciplinary challenge of presenting the example of research method for combining the different technical fields.

Comment (Seigo Kanemaru, AIST)

This paper reports the R&D results at AIST on the 3D stacking technology that is a new method to increase the integration level of the integrated circuit. Although the 3D stacking technology has existed as an idea before, it did not become a main topic of R&D due to the technological difficulty of achieving three dimensional integration, and the integration level of IC was improved through the size reduction of the transistors. Currently, as we recognize the limitation of size reduction, the 3D stacking technology is coming into light again. However, this technology has many issues, and the fundamental technologies must be developed to solve them. I think AIST has taken the strategy to utilize the limited research resource efficiently to work around these issues. I believe if you clearly discuss your efforts from these perspectives in this paper, it will be useful information for those engaging in other research issues where the integration of fundamental technologies is involved.

Answer (Masahiro Aoyagi)

I added the descriptions of the specific strategic efforts for effectively utilizing the limited research resource to tackle the issues of 3D stacking technology, and the priority of issues and the obtainment of research resources, in an understandable, chronological order.

2 Goals

Comment (Naoto Kobayashi)

I can see that you are aiming for systematic development of the 3D IC chip stacking technology in this paper. However, I hope you state what and how much you aspire to realize as practical technology unseen anywhere else, and how the companies can use such new technology. Particularly, you write in Chapter 6, "the final outcome is to provide an R&D environment for design, prototyping, and evaluation that matches the practical system," but if you are setting that as your final goal, I think you should describe what is the realistic output you set as your goal of this research. I think you should state this at the end of Chapter 2, but in that case, I think you should make the title of Chapter 2, for example, "Advancement of the electronic hardware system integration technology by 3D IC chip stacking and the aim of this research."

Answer (Masahiro Aoyagi)

About your indication, "I think you should describe what is the realistic output you set as your goal of this research," I added some descriptions to the end of Chapter 2.

3 Comparison with competing technologies

Question & comment (Seigo Kanemaru)

Please describe in understandable terms, the advantages and disadvantages of the SOC, SIP and 3D stacking technologies that you show in Fig. 1, from the viewpoints of constructing a competitive electronic system. If you can clarify the reasons for the high expectations for the 3D stacking technology that is technologically difficult, I think the readers can more readily understand the value of this paper.

Answer (Masahiro Aoyagi)

Considering the performance, power consumption, size, design cost, manufacturing cost, and others as the indices of increased performance, the 3D stacking technology can be achieved in various combinations (depending on priority given to performance, cost, etc.), and I think it is difficult to compare simple advantages and disadvantages. In this paper, we describe the representative example giving priority to power consumption.

4 Specific fields of application for the 3D stacking technology

Question & comment (Naoto Kobayashi)

Large investment is necessary for the development of general-purpose semiconductor technology, and the technology faces severe competition and the pace of change is fast. You write (in Chapter 2) that the SOC technology is facing difficulties in business for such reasons. If the 3D stacking technology is useful, such high-end technology will be put to practical use in the near future, and similar business issues may arise. On the other hand, I think the functional semiconductor devices that combine sensor, actuator, and others require very special technology, and the TSV is already used in some parts. What is the final form (specific field of application) of the 3D stacking semiconductor that you are aiming for in this research?

Answer (Masahiro Aoyagi)

I added the description in Chapter 5 on the final form (specific field of application) of the 3D stacking semiconductor that we are aiming for in this research.

5 Cost reduction by the 3D stacking technology

Question & comment (Naoto Kobayashi)

The 3D stacking technology is gaining attention around the world, and is already incorporated in stacking SOC and DRAM, but I hear that, in reality, the cost is one of the bottlenecks. In the text (Chapter 2), you write that the cost of development and manufacturing can be reduced greatly by 3D IC chip stacking technology compared to SOC. Please tell us if you have any specific cost estimates or projections for the 3D stacking technology as an advanced SIP technology.

Answer (Masahiro Aoyagi)

For a cost estimate, an accurate one is difficult within the range of information that can be disclosed. I added some general description, and added some source material from a technological survey company in the reference section.