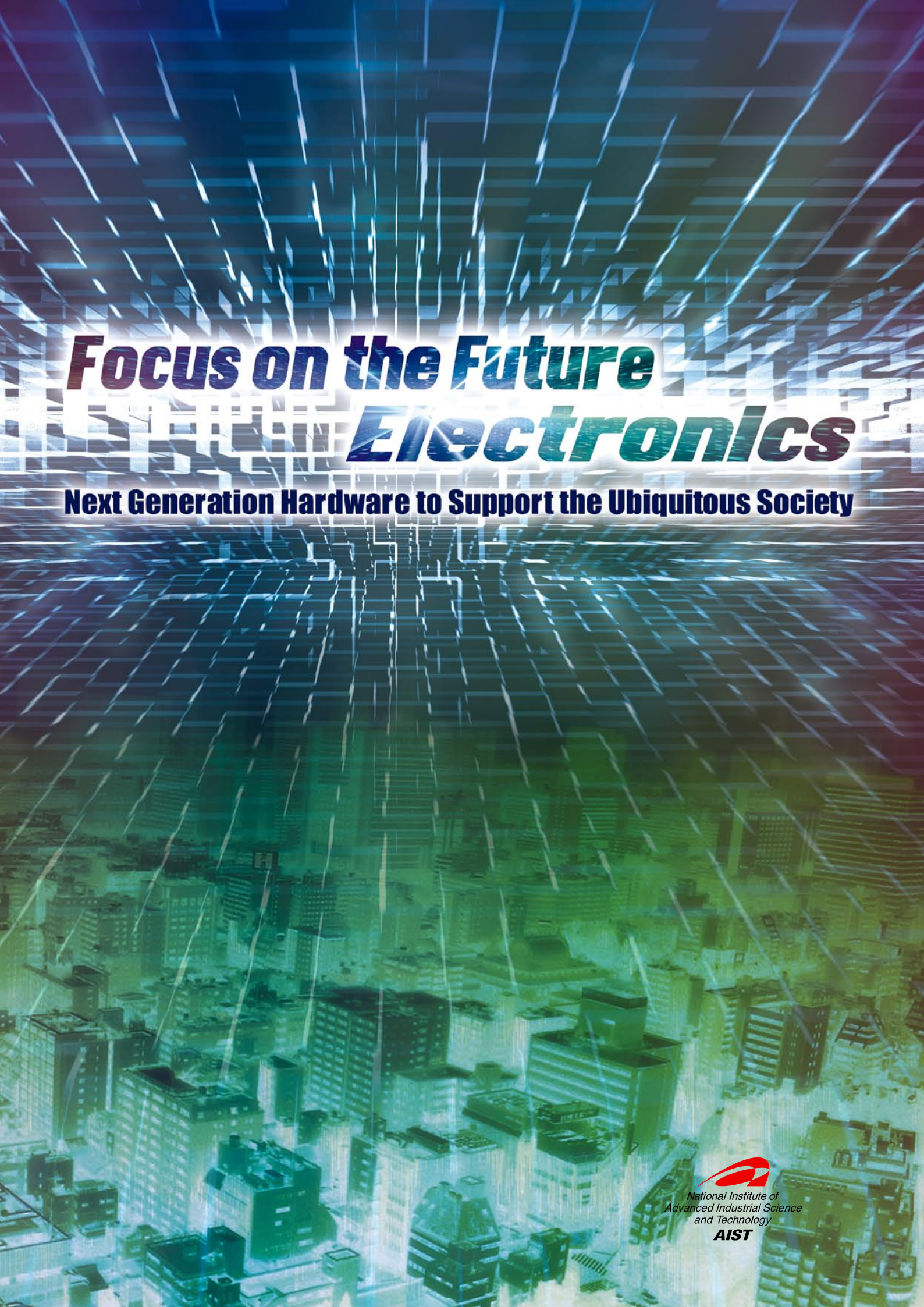
Focus on the Future
Electronics

Next Generation Hardware to Support the Ubiquitous Society



National Institute of
Advanced Industrial Science
and Technology
AIST

To Improve the Performance of All Kinds of Electronic Devices

Humans aspire for the rich, secure IT society. It can be said that the key to the development of the robot industry and of personal mobile electronic products is the development of higher performance, low energy consumption electronic devices. At AIST the development of next generation devices is being performed in various aspects to support the ubiquitous society.

Devices to support the ubiquitous society are required to be small so that they can be installed anywhere, to have low energy consumption so that they can be used even in large numbers and also to be highly functional to satisfy increasingly high level demands.

At AIST, research strategies are decided and research issues are repeatedly discussed. Currently, silicon CMOS is the main technology used in data processing devices but the continuing pursuit of performance improvements in CMOS devices through miniaturization is, because of physical and engineering difficulties, reaching its limit. Together with miniaturization, the introduction of new materials, new transistor structures and new processes, and further improvement of manufacturing techniques, have become indispensable. At the same time, the measurement and analysis technology that supports these has become extremely important.

Also, having the limits of silicon CMOS technology in sight, many devices with different principles of operation from CMOS have been proposed but at present no specific candidate replacing CMOS has been settled upon. Also, difficulties are being pointed out with memories (DRAM, SRAM, flash *etc.*) the capacity of which has increased remarkably. Proposals and development are aimed toward the practical utilization of new forms of high speed, non-volatile, CMOS compatible memory.

As research and development strategies for next generation data processing devices to support the ubiquitous society, when thinking about the above logic circuits and memory devices, three technologies shown in this pamphlet can be considered to play extremely important roles.

The three technologies introduced here are as follows.

First, with regard to silicon semiconductors, which represent the mainstream in current technology, the

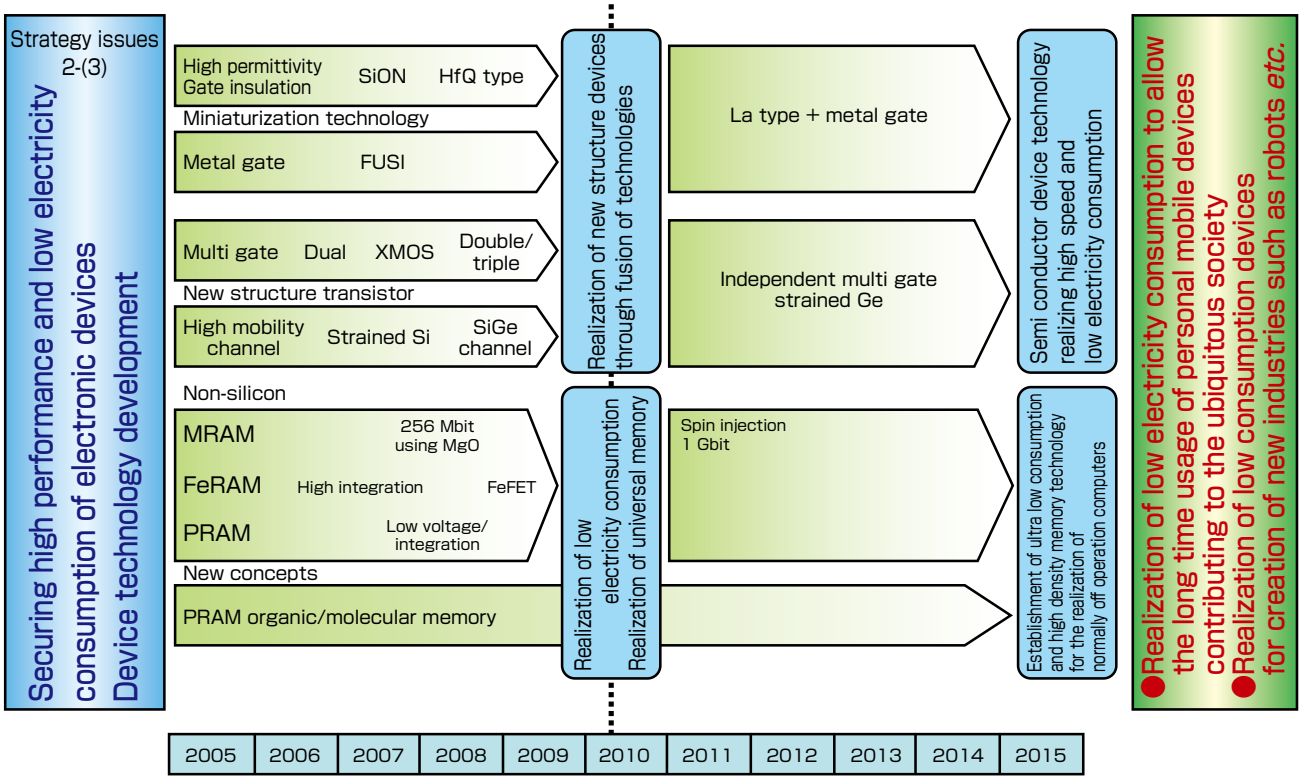


Figure 1 : AIST's device technology roadmap (extract from phase 2 AIST research strategy)

results of size reduction, low electricity consumption and high level functionality research at the Advanced Semiconductor Research Center are presented. Next, research on XMOS transistors, which aim at high speed with the introduction of a new gate structure, is explained. Thirdly research regarding memory which retains data even after the power supply is turned off is presented. The last two researches are mainly pursued in the Nanoelectronics Research Institute.

Figure 1 shows an extract of in the information technology and electronics field, the roadmap relating to electronic devices. The part labeled "Semiconductor device technology to realize high speed & low electricity consumption" in the upper half of the diagram shows the roadmap corresponding to the silicon semiconductor research pursued by the Advanced Semiconductor Research Center together with the Ministry of Economy, Trade and Industry and to the XMOS research being pursued by the Nanoelectronics Research Institute. The section labeled "Establishment of ultra low consumption and high density memory technology for the realization of normally off computers" in the lower half corresponds to the roadmap for non-volatile memory research pursued at the Nanoelectronics Research Institute.

At AIST, there is a super clean room (SCR Bldg.) maintained by the Advanced Semiconductor Research Center together with industrial companies, a clean room at Nano materials Bldg. The device development phase being carried out at these facilities is shown in Figure 2.

At the SCR Bldg, mainly the Advanced Semiconductor Research Center, is doing research to make current silicon semiconductors smaller, faster and lower in electricity consumption. And in Nanomaterials Bldg. research into next generation technology is carried out.

By making the facilities, especially SCR Bldg., open for use by companies and universities, AIST hopes to fulfill the role of "knowledge concentration center" for a semiconductor device technology. We are discussing the issues with related parties. AIST aims to function as a "hub" to bring about innovation in the IT society, constructing a world leading knowledge base system for the nanoelectronics field and setting as its goal contribution to the continuing development of the electronics industry. For example, as a technology system for pursuing the limits of CMOS miniaturization, AIST aims to construct a base system that can be used to predict and analyze device properties, by combining, technology for devices with new materials and new structures, process technology, measurement/analysis technology and *ab initio* simulation. This knowledge base system is to be called the nanoelectronics innovation platform (NIP). Using NIP, demonstrational research based on the creative ideas produced by universities, industry and independent research institutions will be performed and the possibility of further development will be assessed, leading to full scale research and development.

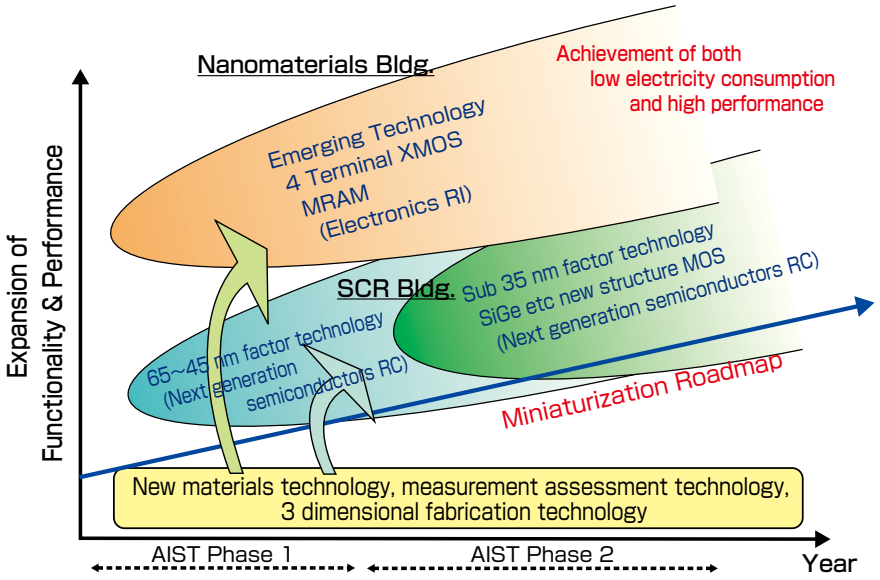


Figure 2 : AIST clean room device development phases (extract from AIST phase 2 research strategy)

I hope that this pamphlet will be of help to the nation's semiconductor research.

Research Coordinator
(Information Technology & Electronics)
Kazuhito Ohmaki

MIRAI Project Builds the IT Society

The role of electronics

With the progress of communications technology, people have become able to use various network services without restrictions on time and place. In order to ensure the convenience and safety of living space in ubiquitous society, the role of electronics systems is becoming more and more important.

The core technology of digital home appliances, cellular phones and automobile electronics *etc.* is that of semiconductor device such as processors and memory (Figure 1). For this reason, the cost and performance of semiconductors determine the added value of many of these products.

The domestic semiconductor market is ¥5 trillion, representing around 1% of the GDP, but it is said that the extent of its knock on influence, including displays, automobiles, industrial machinery and medical equipment *etc.* amounts to ¥200 trillion (40% of the GDP). It can be said that there is a direct connection between the competitiveness of the semiconductor industry in the world market and the international competitiveness of Japan's manufacturing industry.

One chip semiconductor for advanced information processing – the source of industrial competitiveness

Semiconductors that perform wireless communication and image/sound processing and recording *etc.* have from several tens of millions to in excess of several hundreds of millions of transistors integrated on around a 1 cm^2 area of silicon chip.

As shown in Figure 2 (left), memory and processors are integrated onto a semiconductor chip, with the functions of the various integrated circuit blocks structured to operate in concert. Figure 2 (right) shows the processing capabilities of media processors for various media such as high definition TVs. Although these are specialized processors, they have around the same level of processing capability as general purpose processors such as Pentium.

Figure 3 shows a cross section of the structure of the MOS transistors used in current integrated circuits (left diagram). Regarding gate length and gate insulator film thickness, the corresponding parts have come to occupy areas of extremely minute dimensions (right diagram). Because of miniaturization, the structure of current transistors results in an increased leak current and the problem now faced is that the drive current, which determines transistor performance, cannot be increased any further. In order to overcome this problem, two main solutions are being considered, as shown in Figure 4.

One solution is to change the transistor structure from a planar structure to a three dimensional one and the other is to add a strain to the Si of the channel, so that the current can flow more easily or to change the material from Si to Ge so that the drive current can be increased. Research and development is proceeding in these areas. In addition, a lot of research is being carried out into replacing conventional SiO_2 used in the gate insulator film with a high permittivity (high-k) material.

In the 60 years since the transistor was invented and the 50 years since the integrated circuit was invented, the performance and data processing capabilities of semiconductors have rapidly improved, revolutionizing and developing the information society. However, improving performance by miniaturization of transistors alone, as has been the case up until now, has become difficult and the introduction of new structures and new materials has become necessary. This is the reason that the history of semiconductor technology has now reached a great turning point.

The reason new semiconductor technology development is being so energetically pursued by the world's semiconductor industry, public research organizations, universities and consortiums *etc.* is that winning through in the coming competition to develop technologies will lead to the strengthening of the basis securing their continued existence, and also enriching the source of national industrial competitiveness.

Digital Home	Media Processor, Display
Mobile/Broadband	Multiprocessor/Core, NAND Flash Memory
Digital Car	Engine Control, Driving Support System

(Unit:Yen)

	Japanese Market	U.S. Market	World Market
Semiconductor Devices	5 trillion	12 trillion	25 trillion
Displays	2 trillion	—	6 trillion
Automobiles	40 trillion	40 trillion	200 trillion
Electronic Equipment	23 trillion	—	120 trillion

Establishment of sustainable technological supremacy and strengthening of new market creation capabilities through new technology are necessary.
Impact of the semiconductors on GDP is ¥200 trillion (40% of ¥500 trillion GDP).

Figure 1 : Semiconductor devices in the ubiquitous society

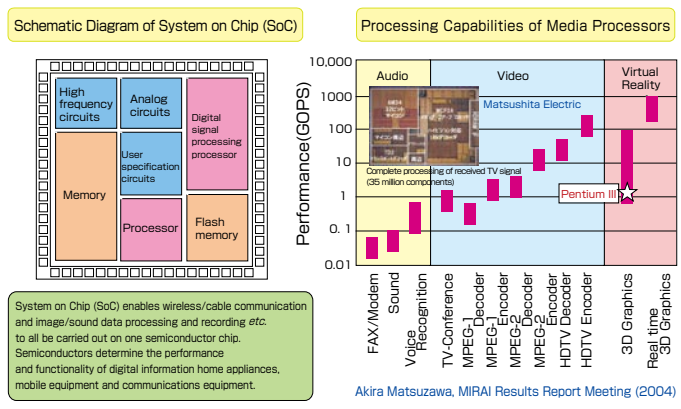


Figure 2 : Semiconductors that perform advanced data processing

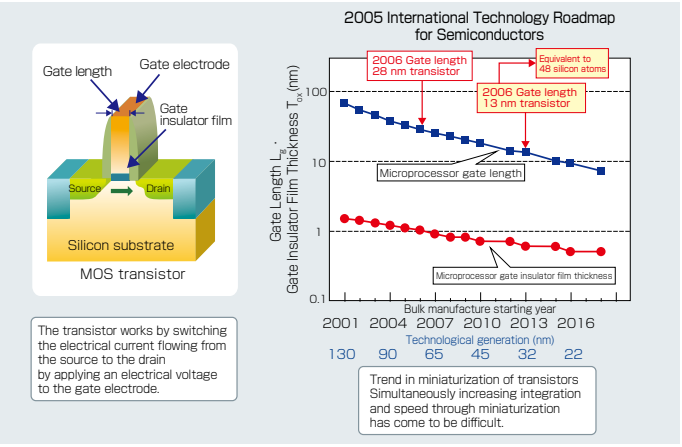


Figure 3 : Miniaturization towards a 10 nanometer gate length MOS transistor

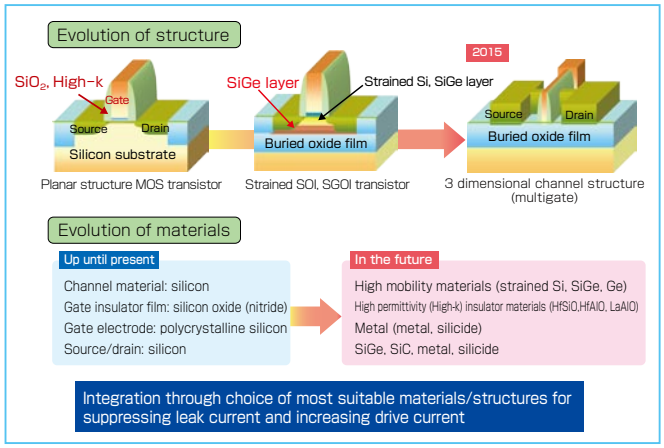


Figure 4 : New materials and structures aimed at improving transistor performance

AIST and semiconductor research

AIST's semiconductor research started soon after World War Ⅱ while in its previous form as the Electrical Laboratory (and later as the Electrotechnical Laboratory) by Michio Hatoyama, Makoto Kikuchi and associates. In the early 1960s integrated circuit research began with Yasuo Tarui at the center. In 1967, Tarui *et al.* performed development of electron beam lithography equipment. In 1976 – 1979, the VLSI Technology Research Association was formed with the purpose of competing with IBM's new computer system "Future System". As a 4-year government subsidized project with a research budget of ¥72 billion (of which ¥30 billion was subsidy), a large scale national semiconductor project was carried out with government and private sector cooperating as one to tackle research and development. The results of this national project afterwards supported the rapid growth of the Japanese semiconductor industry in the 1980s. Also, during this period, the original model for the current double gate MOS, the XMOS, was invented by Yutaka Hayashi *et al.* at the Electrotechnical Laboratory in 1982. The Japanese semiconductor industry, which achieved great success centering on semiconductor memory (DRAM) in the 1980s, has, from the last half of the 1990s onwards due to competitive pressure from various Asian countries, been gradually forced into a hard fight within the world market.

Semiconductor MIRAI Project

Given this situation, in order to restore the competitiveness of the national semiconductor industry, the 7 year "Millennium Research for Advanced Information Technology (MIRAI) Project" of the New Energy and Industrial Technology Development Organization (NEDO) was started in 2001, As a base for the focus of research by industry, academia and government, the Super Clean Room (SCR Bldg.) was completed at AIST Tsukuba at the end of FY 2001. MIRAI Project research and development is currently proceeding, with the participation of AIST and university researchers together with company researchers transferred via ASET (Association of Super-Advanced Electronics Technologies), forming a cooperative research body with the SCR Bldg. as its base of operation. From August 2001, with 120 industry, academic and government researchers and adopting a centralized research system with 5 research themes, phase 1 (2001-2003) and phase 2 (2004-2005) research proceeded (Figure 5). In the 5 years up until the end of phase 2, a total of ¥22.5 billion was expended on research and the technology resulting from the research and development done in this period was transferred to the MIRAI participant corporations, Selete (Semiconductor Leading Edge Technologies, Inc.) *etc.* at the end of FY 2005. Research is currently continuing for technology transfer of certain parts of the results.

Today, the issues that present barriers to semiconductor technology development all require a return to technological basic principles in order that proposals can be made for methods to overcome physical limits and that measures to scientifically prove the validity of these proposals are taken. The basic philosophy of the MIRAI project is to realize technological breakthroughs through the close cooperation between science and technology. Base technologies necessary for this, such as materials, processes, equipment and inspection/measurement methods have been developed within the project.

Three research themes: low-k material interconnect module technology, lithography related measurement technology and circuit system technology (Figure 5), concluded at the end of FY 2005, have reached their targets. Technical

results were transferred to material makers, device makers and consortiums (Selete) *etc.* (see table).

Presently, the results of mask defect inspection technology development are being converted to commercial use by an equipment maker. Results from the development of the critical dimension atomic force microscope, which can measure 3 dimensionally the size and shape of the fine patterns on silicon wafers at high accuracy on the sub-nanometer level, are planned to be commercialized by an equipment maker within a year. Two material makers are aiming to commercialize the newly developed ultra low-k material for use in Cu interconnects, and have taken on responsibility for supplying samples to Selete and device makers.

High-k gate insulator film fabrication technology has been transferred to an equipment maker where it has already been turned into a project. The technology was also transfered to Selete.

In MIRAI project phase 3 (2006-2010), new themes, entrusted by NEDO to Selete, are added and a new organization has been formed with an AIST/ASET joint research body and Selete pursuing 6 research themes (Figure 6). The U-CMOS research and development pursued by AIST/ASET is scheduled for completion within FY 2007 as initially planned. As part of this, the new transistor structure related technology has developed on the results of phase 1 and phase 2. It succeeded in the development of a uniaxial strained fin type transistor (a fusion between a double gate MOS transistor and a strain effect transistor) that realizes high performance CMOS technology (Figure 7). Prototype of this device has been fabricated with the full cooperation of device makers participating in MIRAI Project. Through the know-how accumulation in the research and development process of makers, the technology will be transferred more effectively.

With extreme miniaturization, the ability to measure the distribution of impurities such as donor, acceptor *etc.* in device regions with the atomic scale resolution, and the measurement of localized "stressed" regions in transistors have become indispensable. MIRAI Project has

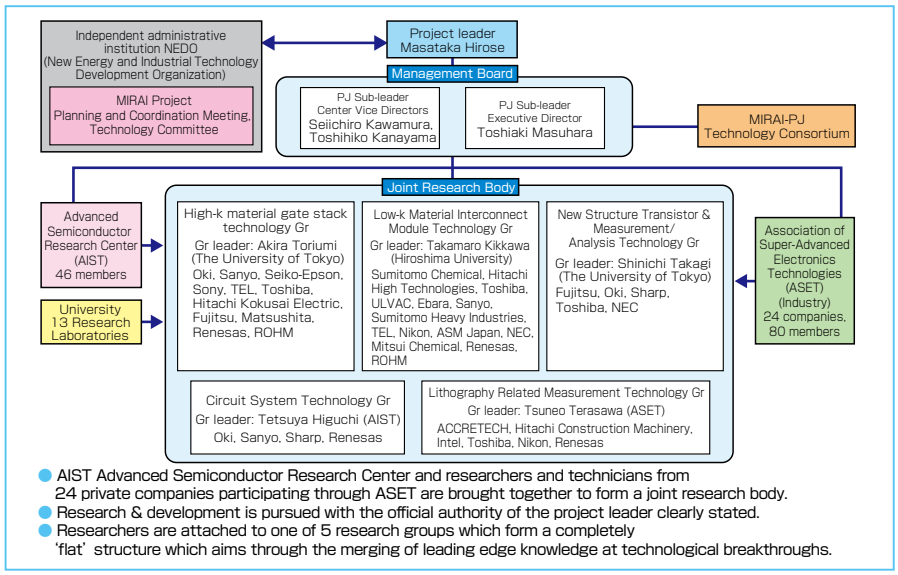


Figure 5 : MIRAI Project Research and Development Structure (2001-2005)

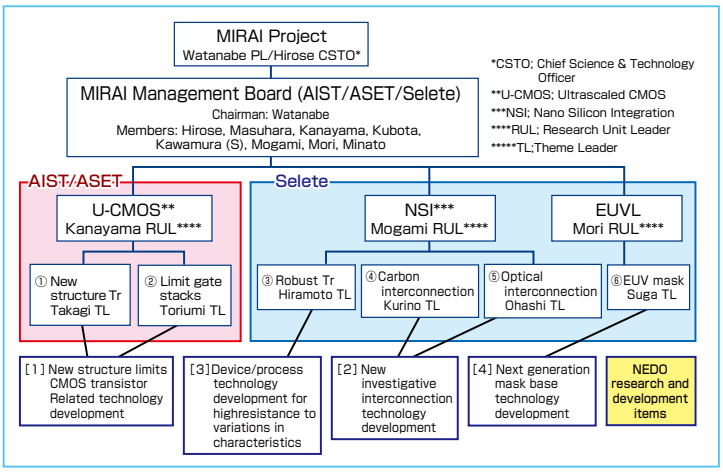


Figure 6 : MIRAI phase 3 management system

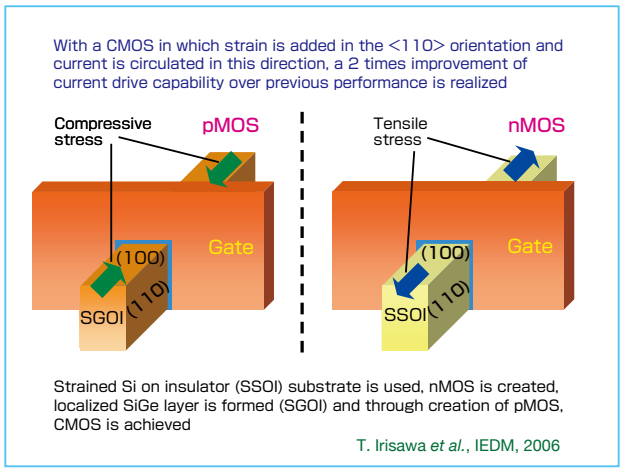
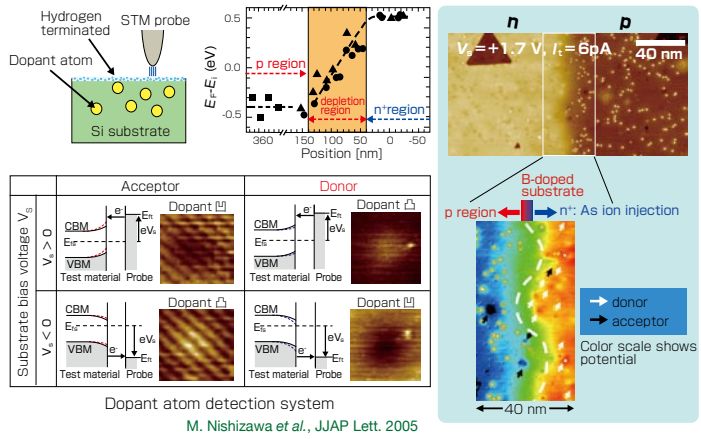
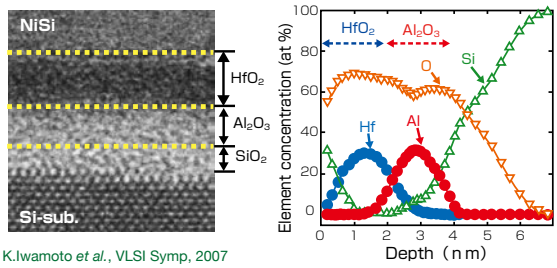


Figure 7: Most effective structure for uniaxial strained multigate CMOS (modulation of sub-band structure)



M. Nishizawa *et al.*, JJAP Lett. 2005

Figure 8 : Detection of individual impurity atoms in a Si crystal and simultaneous potential measurement by STM



K.Iwamoto *et al.*, VLSI Symp, 2007

Figure 9 : Cross-sectional transmission electron microscope photograph of high-k gate insulator film consisting of a gate stack comprised of 2 layers: HfO_2/Al_2O_3 (left), and profile of composition of $HfO_2/Al_2O_3/SiO_2$ layers by depth

It was thought that MOS threshold voltage was determined by the characteristics of the upper interface between the NiSi (gate electrode) and HfO_2, but it is now understood that this is determined by the Al_2O_3 and SiO_2 lower interface multi atom layer region. The same conclusion was reached even when the positions of the upper HfO_2 and lower Al_2O_3 layers were swapped over. This discovery, which overturns the popularly held academic view, will change CMOS design methods.

led the way in the development of these technologies (Figure 8). The problem of variations in device characteristics will become increasingly pressing. In order to determine the reasons for the variations, it is necessary to accurately understand the behavior of dopant atoms under heat treatment, behavior of localized strain in transistor active regions and the local fluctuations in gate length, and nanoscale spatial resolution measurement is becoming increasingly important.

Also, with regard to extremely high-k gate stack technology development, a basic principle for designing the metal gate and high-k materials as one body in order to control the transistor threshold voltage has been newly established (Figure 9). This is a new discovery that will force a fundamental re-evaluation of the academic thinking on the subject that has existed up till now. The demonstration of these kinds of new concepts has been made possible because prototype equipment that can control growth of high-k thin films on the atomic scale has been developed in MIRAI Project. It will not be long before a complete system encompassing equipment, materials and device technology appears for the purpose of designing and manufacturing high-k gate stack structures based on high-k MOS transistor threshold voltage basic control principles.

It is expected that these results will be widely developed for application in the semiconductor industry and will create innovation in device technology.

Table : Technology transfer of MIRAI development results to industry

● Research and development adjusted to development application schedules of device makers at the top of the industry

MIRAI results (new concepts, top in the world)	Destination of 1st transfer (application development, industrial project)	End user
Lithography related measurement: Mask defect inspection factor technology	Toshiba/NuFlare (equipment project)	Mask maker, Device maker
	Selete (joint development)	
Lithography related measurement: Miniaturized pattern 3 dimensional measurement technology	Hitachi Construction Machinery (equipment project)	
Lithography related measurement: Wafer pattern defect inspection technology	ACCRETECH (equipment project)	
Lithography related measurement: EUV mask blanks defect inspection technology	Selete (practical machine development)	
Low-k: Ultra low-k material technology	ULVAC/Mitsui Chemical (material project)	Device maker
Low-k: Interconnect formation process technology	Selete (interconnect module development)	
Low-k: Plasma polymer low-k material technology	NEC (joint research)	NEC Electronics
High-k: Material deposition technology	Hitachi Kokusai Electric (equipment project)	Device maker
High-k: MOSFET threshold voltage technology	Selete (deposition process development)	
New structure transistors: Strained Si, SiGe wafer technology	Toshiba Ceramics/Komatsu Electronic (joint research)	Device maker
Circuit systems: TCAD parameter automatic extraction technology	Selete (joint research)	Device maker

Advanced Semiconductor Research Center
Masataka Hirose

LSI Technology Aims to Be a New Direction for Development

Obstacles to further miniaturization

Silicon large scale integrated circuits (Si LSI) support the hardware side of the IT society. The remarkable development of LSIs has been achieved through miniaturization of device dimensions (scaling) of MOSFETs (metal-oxide-semiconductor field-effect transistors: single-gate MOSFETs on a Si bulk substrate) of which LSI circuits are composed so far. At present, the semiconductor technology generation (technology node) has already reached the 65 nanometer generation level. It can be said that LSI technology has become a major part of the nanotechnology.

At the same time, we are forced to recognize the strong awareness that extremely large obstacles stand in the way of continuing to reduce the dimensions of devices in order to increase functionality and level of integration as has been done up till now. In other words, we are starting to notice the misgivings that the miniaturization will result in the short channel effect and increase in the leak current, which causes degradation of switching characteristics and prevent the expected improvement in device performance.

XMOS devices breaking through the barrier of miniaturization

As a device structure to solve those intrinsic problems, a double gate MOSFET (initially named XMOSFET, after the Greek letter Ξ (X in the English letter) that resembles the shape of the cross section of the device) with a top-and-bottom gate, was proposed by the Electrotechnical Laboratory (now AIST), in 1984.

The double-gate structure firmly shields the channel from the drain field, and the effect of the drain on the source is kept minimal. Thus the limit on the bulk MOSFET miniaturization can be exceeded. Afterwards, in the late 1990's, the scaling limit of silicon devices began to emerge as a practical problem. Then the effectiveness of the double-gate structure was evaluated and the latest edition (2005) of the ITRS (International Technology Roadmap for Semiconductors) cited the double-gate MOSFET as an ultimate MOS device.

In 2001, AIST took up the XMOS technology as one of the priority themes, and aimed to establish the XMOS device fabrication technology through the development of original processes such as an anisotropic wet etching (Figure 1), a neutral beam etching and an ion bombardment retarded etching *etc.*

Misgivings regarding increase in the leak current (inactive power)

Another serious problem equal to or greater than the miniaturization issue

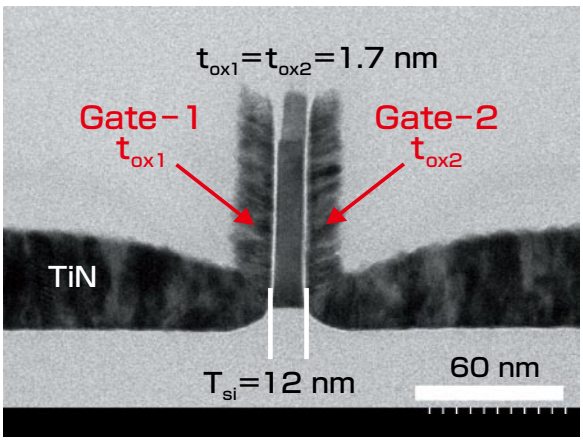


Figure 1 : Prototype 4-terminal double-gate MOSFET (4T-XMOSFET)
Fabricated by using the anisotropic wet etching for the well standing-up fin channel, and the reactive ion etching (RIE) for the gate separation.

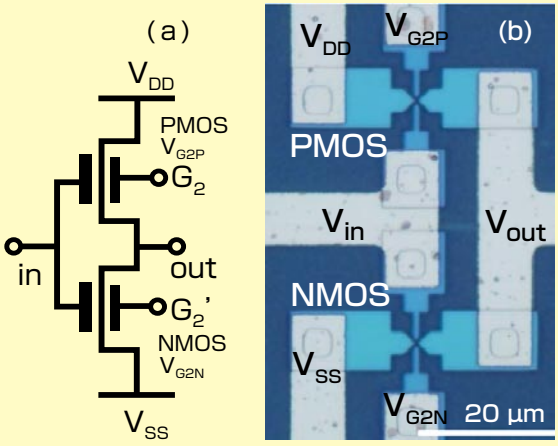


Figure 2 : CMOS inverter that uses 4-terminal double-gate MOSFETs (4T-XMOSFETs)

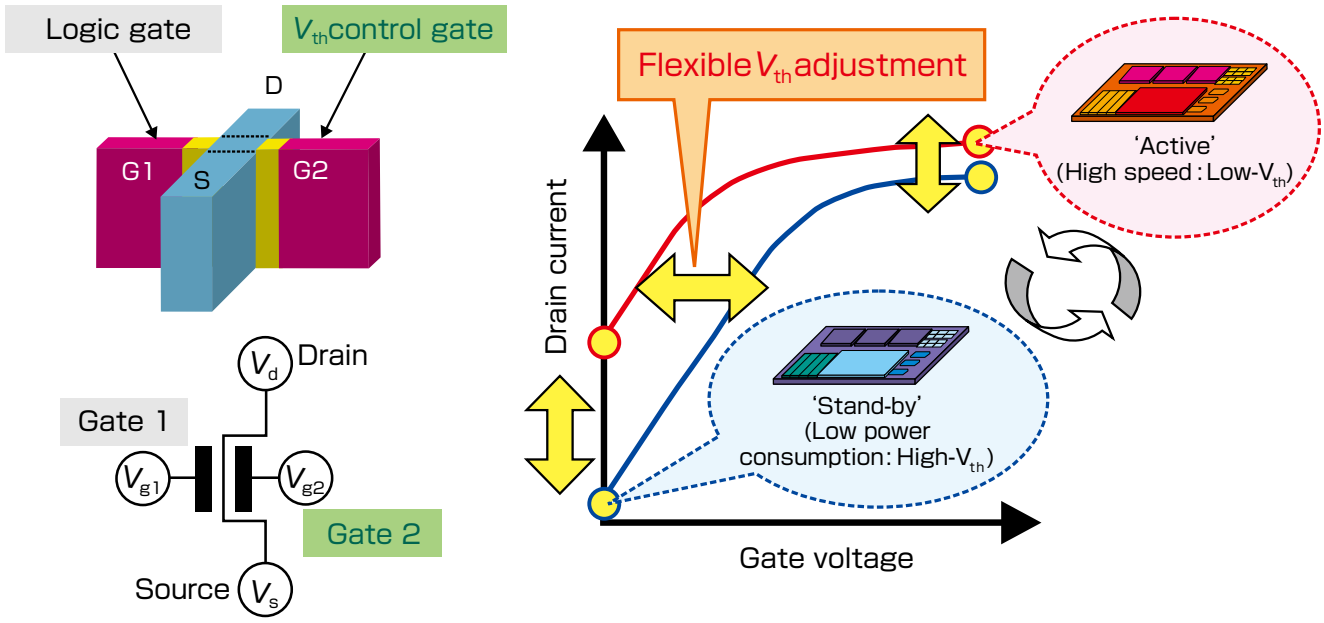


Figure 3 : Unique function of the 4-terminal double-gate MOSFET (4T-XMOSFET) By flexibly controlling V_{th}, both high speed during the active state and low power consumption during the standby state are achieved.

is the increase in the inactive power due to the leak current. The transistor threshold voltage V_{th} is closely related to performance and energy consumption of LSIs. In order to raise speed, namely drivability, it is necessary to choose a low V_{th} value and increase the ON current I_{on}, which also causes the increase in the standby leak current and inactive power.

Conversely, the standby leak current can be reduced by raising V_{th}, but at the same time the ON current is also reduced and the operation speed cannot be raised. This situation is the same for both the bulk MOSFET and double-gate MOSFET with a usual common gate, because the threshold voltages are fixed in both cases.

New LSI "hot & cool chip"

In contrast to the above-mentioned situation, if the double-gate is separated and two gates can be driven independently, one gate can be used to perform switching and the other one can freely control the threshold voltage V_{th}.

Therefore, in the active circuit state, the drivability can be increased by raising the ON current, and during the standby state the OFF current can be decreased and the stand-by inactive power is drastically reduced. Thus an ideal circuit operation is able to be achieved (Figure 2).

If the four-terminal double-gate MOSFET (4T-XMOSFET) as an advanced XMOS device with such a new function is used, it is expected that a ultra low-power consumption LSI having optimum power control, in other words, a "hot & cool chip", can be realized (Figure 3).

It can be said that the ubiquitous electronics (electronic devices that allow us to enjoy the benefits of the IT technology anytime and anywhere) will drive the IT society, where both the advanced data processing function and the low energy consumption are necessary. Therefore, we believe that LSIs composed of the 4T-XMOSFETs will play an active part in near future.

Nanoelectronics Research Institute
Eiichi Suzuki

Nonvolatile Memory that Gives Ultra Low Electricity Consumption

Nonvolatile function and the ubiquitous society

The vast amounts of content data that are transferred across the internet, such as movies and music, are stored on hard disk servers. The mobile music players that are necessary items for enjoyment of music are achieved by using flash memory. In both of these electronic devices data is not lost even if the power is turned off (non volatility). The demand for nonvolatile devices in various areas is increasing.

In order to store the explosively increasing volume of data, further increase in the data storage capacity of hard disks is indispensable. Also, for the movie data, the amounts of data around a thousand times larger than that of music data, the operating speed of flash memory is too slow. The fact that flash memory breaks after usage of several tens of thousands of times confines the possibilities of nonvolatile memory. If high speed, high capacity and nonvolatile memory that can be written and read unlimited number of times (universal memory) could be achieved, computers that can be used at the moment their power is turned on would be possible. If logic devices also come to have nonvolatile functionality, still greater developments can be expected.

With current silicon semiconductor logic circuits, it is necessary for the power to be continuously switched on in order to preserve data. If nonvolatile logic devices could be created which do not lose data even if the power is switched on and off several thousand times per second, then it would be possible to make computers which to human beings look as if they are continuously operating, but in fact have their power switched off for most of the time. This is expected to yield dramatic reductions in power consumption. We have named these “normally off computers” and have made them our long term goal.

Spintronic technology using the ultimate microscopic magnets

Ferromagnetic materials are the most suitable for the achievement of nonvolatile memory. Their speed and their ability to be written and read an unlimited number of times have already been proven by hard disks.

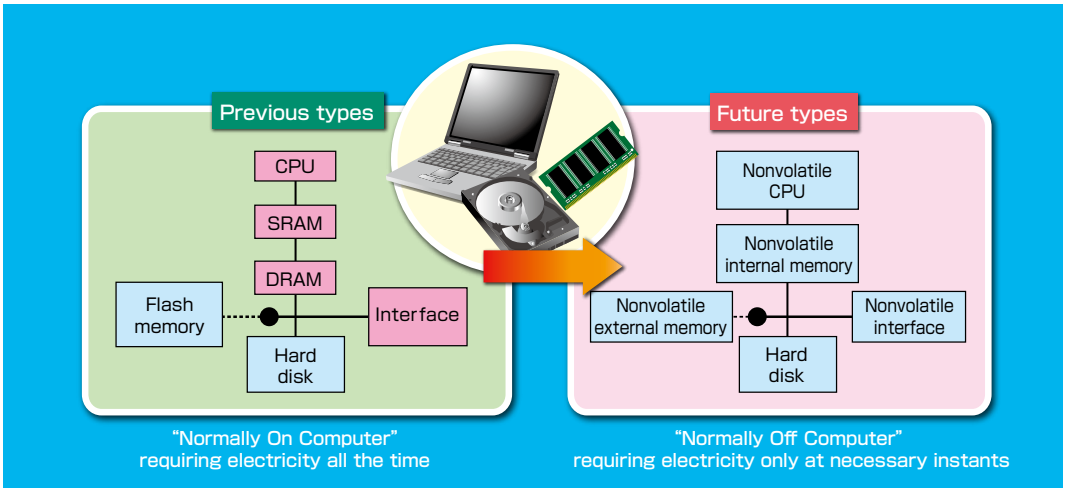
However, for use within electric devices, a conversion between magnetic and electric data is necessary. For a long time, coils have been used for this purpose but their conversion efficiency is low and the limits for improvement have been reached.

The new technology called spintronics solves this problem. Using this technology, conversion between magnetic and electric data can be carried out at high efficiency without the use of coils.

Each electron that carries electric currents has the characteristics of an extremely small magnet (spin). In particular, the electric current which flows out from ferromagnetic materials represents a flow of small magnets with their magnetization direction aligned in the same direction. This spin current can only be observed very closely to the ferromagnetic material (within about 10 nanometers) and so using it has not yet been possible.

However, nanotechnology has made it possible.

Of the consequent results, the most worthy of attention are the tunnel magnetoresistance (TMR) devices. These are devices consisting of a combination of



If nonvolatile devices, which do not lose their data even if the power is turned off, can be developed, then a great reduction in the electricity consumption of electronic data devices is expected.

thin ferromagnetic films and an insulator film of thickness in the nanometer range.

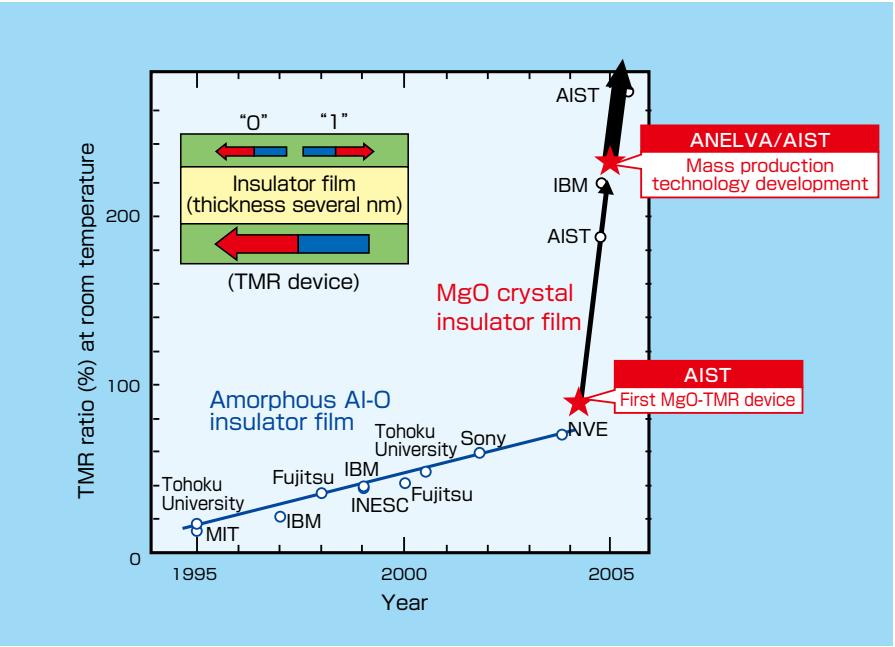
The amount of the spin current passing through the insulator film changes depending on the direction of magnetization of the ferromagnetic films. By using this phenomenon, magnetic data can be read electrically without the use of a coil. Performance is indicated by the resistance change ratio (TMR ratio).

In 2004, we developed a completely new TMR device using MgO crystal as the insulator film and achieved a big leap in performance. Teaming up with a manufacturer, we also succeeded in developing mass production technology. By including MgO-TMR devices in hard disks, a large scale increase in storage capacity can be achieved. This technology has been already included in hard disk drives worldwide.

MgO-TMR devices also represent a powerful card in the development of universal memory. Increasing the capacity of nonvolatile MRAM, which uses ferromagnetic material, was considered to be difficult on 2 points of read signals and write power. With the appearance of MgO-TMR devices the read signal problem has been completely solved.

All that remains is the write power problem. As before, MRAM uses coils for this purpose. We are currently developing a new type of MRAM (Spin RAM) that uses spin current to write magnetic data in place of a coil.

Also, aiming towards nonvolatile logic devices, we are currently developing spin transistors, which utilize the injection of spin from ferromagnets into semiconductors and ferromagnetic semiconductors, which turn the semiconductor itself into a ferromagnet.



History of the performance improvements of tunnel magnetoresistance (TMR) devices which convert magnetic data to electric data
AIST created a new type of TMR device which uses MgO as the insulator film.

Aiming to produce a "normally off computer"

Spintronic technology will lead to the realization of mass storage, universal memory and also a new type of data communications equipment *i. e.* a normally off computer. Following the first appearance of the microprocessor, there was a proposal to help Africa by combining solar cells with small computers, but even after 30 years this is still to be realized.

With the ultra low electricity consumption provided by nonvolatile devices many dreams like this, which are still to be fulfilled, can become reality.

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Focus on the Future Electronics

Next Generation Hardware to Support the Ubiqutous Society

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