The miraculous development of the performance and integration density of silicon ULSIs composing the latest information and communication devices has achieved as a result of the minituarization of MOSFETs. However, major obstacles are expected to stand in a direct challenge to further miniaturization for further integration. The biggest hurdle to the further miniaturization is the short-channel effect, i.e., the mutual interference between the source and drain as the distance between them is reduced. This results in a degradation of the device performance, thus determining the limits of minituarization. Although the double-gate MOSFET, wherein a thin channel is layered between two gates, has been recognized as the ultimate device structure in order to eliminate this problem (See International Technology Roadmap for Semiconductors 2001). X MOSFET, the double-gate MOSFET, proposed by the former Electrotechnical Laboratory for the first time in the world has not yet been put into practical application due to the difficulty of fabrication of the double-gate structure. However, the double-gate MOSFET has rapidly received much attention in the U.S. as a future device since 2000. The development of a Fin-type double-gate MOSFET (the double-gate MOSFET where the drain current horizontally flows through the Si Fin channel, see Fig. 1, center) has been
The device's two-gate structure permits optimal control of threshold voltage, which makes it possible to minimize the power consumption. In this sense, the double-gate MOSFET is very promising as a solution to another problem inherent to ULSI, that is, desperate increase in power requirement.

The new vertical double-gate MOSFET developed by AIST utilizes a commercially available bulk Si substrate. Fabrication of the world's thinnest channel was achieved by using the conventional CMOS fabrication technology and the newly discovered process where an etching rate by an alkaline solution is greatly retarded at the surface exposed to ion bombardment. With this new process, the group has succeeded both in fabricating a prototype of the world's thinnest vertical double-gate MOSFET featuring a channel thickness of 15 nm and in providing the experimental proof of its double-gate performance. Actual measurements confirmed the superior electrical characteristics predicted by the theoretical evaluation. It can be said that this technology paves the way to the practical application of the double-gate MOSFET, or what is referred to as the ultimate MOSFET. These results were presented at the 2002 IEEE International Electron Devices Meeting (2002 IEDM) in December 2002 and generated great interest.

### Newly Developed Ion-Bombardment-Retarded-Etching Process

The technological breakthrough in forming the extremely thin Si wall that acts as a vertically oriented channel is the newly discovered ion-bombardment-retarded-etching phenomenon (patent pending). The commercially available alkaline developing fluid (2.38% tetramethylammonium hydroxide) causes a significant retard in the etching rate for the Si substrate portions exposed to ion bombardment. Using these surfaces as etching masks, the group successfully formed a nanoscale Si wall on a bulk silicon substrate that serves as a vertically-oriented channel. Firstly, a somewhat thicker wall with SiO2 mask was fabricated on a (110)-oriented Si substrate (Fig. 2 (a)). Secondly, 30keV As ions were implanted, where the top and the bottoms of the Si wall were exposed to the keV ions, while the sidewalls remained unexposed (Fig. 2 (b)). When the Si wall is dipped in a TMAH solution, the ion-exposed region worked as an etch-stopper and the Si wall was horizontally etched, ensuring a high level of control of the Si wall thinning. This method is excellent in both repeatability and practicability, enabling it to easily fabricate a Si wall channel thinner than that achieved using lithography without any RIE damage. In fact, this method has been applied to the development of the fabrication process of a vertical double-gate MOSFET (IMOSFET) with an ultrathin Si wall channel.

### Verifying Excellent Device Characteristics

A cross-sectional TEM image of the world's thinnest IMOSFET is shown in Fig. 3. The Si wall thickness is measured to be 15 nm. The operation of the fabricated IMOSFET was verified and the experimental characteristics were precisely measured. Fig.4 shows the dependence of the gate threshold voltage ($V_{th}$) and subthreshold slope (S-slope) on the Si channel thickness, both of which are the important indicators of the performance of the MOSFET. S-slope is
the necessary gate voltage when a drain current increases by one decade in the subthreshold region. The theoretical S-slope at room temperature is 60mV/decade. The prominent short-channel effects are the increase in the S-slope which means degrading drain current stand-up against a gate voltage and the threshold roll-off to the negative direction in case of n-channel. These effects can be effectively diminished by thinning of the Si channel, thus proving the superior characteristics of the double-gate MOSFET. It can be concluded, therefore, that the short-channel effects are sufficiently suppressed by making the Si-channel thickness less than 20nm as shown in Fig.4. This means that the characteristics of the device do not degrade but is rather improved by further scaling-down of the circuit elements. The finding is certainly a major advance in the realization of ultra-high density ULSIs in the future. The experimental results of the fabricated IMOSFET indicate that the S-slope degradation can be effectively inhibited even in the device with a ultra-short channel, meaning that less drain current is required to turn on the device. Hence, the device contributes to less power consumption while the system is in operation. Furthermore, each of the two gates can be utilized to control the gate threshold voltage of one another. This function to optimally control the threshold voltage is an advantage for the power reduction.

Future Prospects

These results have led to the establishment of a basic fabrication technology for scaled vertical MOSFETs(IMOSFETs) using a bulk silicon substrate. The newly developed IMOSFET fabrication technology has the following strong points and is expected to be applied to practical use: (1) utilization of ion-bombardment-retarded etching process to fabricate the thinnest Si wall without any process damage; (2) fabrication of a thinner wall than using lithography; (3) easy scaling to the level of nm by controlling the height of the Si wall; (4) a vertically shaped channel capable of carrying a high electric current; (5) allowing the introduction of a High-K gate dielectric material.

Future plans include improving device characteristics through optimization of the processes, establishing ULSI technology for ultra-low power, and multiple applications of the device, making the most of the features of the double-gate MOSFET as a 4-terminal device.

Further Information

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