R&D of SiC semiconductor power devices and strategy towards their practical utilization

— The role of AIST in developing new semiconductor devices —

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The realization of SiC semiconductor power devices has been highly expected to contribute to energy saving, however, it requires overcoming various technological barriers. AIST has been contributing to this objective for more than 15 years mainly through participation in national projects. Corresponding to the changes of organization of the institute, in this paper, R&D activities for the past years are described in three parts, i.e., 1) the R&D targets, 2) the major issues and strategies for overcoming them and the main results, 3) the evaluation of the validity of the strategies, and lastly, future issues are suggested.

***Keywords* :** Silicon carbide, wide-gap semiconductor, wafer technology, power semiconductor device, power electronics

1 Introduction

At the 15 institutes under the former Agency of Industrial Science and Technology that was the precursor of the current National Institute of Advanced Industrial Science and Technology (AIST) in the 1990s, majority of the researchers were material researchers. In the long-term material research, how we can present our importance to society was a subject of frequent discussions. In the late 1980s, the United States was experiencing economic slowdown, and the American basic researchers were visiting Japan to sell their research. The Japanese national research institutes at the time were in the phase of "shift to basics" or putting emphasis on leading-edge basic research. Some material researchers armed with their specialties engaged in the study of whatever material that was in vogue at the time. At the Electrotechnical Laboratory (ETL), a consciousness shift was promoted under the concept "material is useful only when it is used". The ETL was being left behind in the state-of-art technological development of silicon LSI, but was starting a series of pioneering R&D in the field of materials. It was concluded that to study the material group with prospects for practical utilization in future electronic devices, emphasis should be placed on the wide-bandgap semiconductors such as silicon carbide (SiC) as well as gallium nitride (GaN) and diamond that were expected to achieve low-loss high-frequency operation and high-temperature high-radiation resistance (Fig. 1).

In this paper, the development of the SiC semiconductor power device and the activities toward its practical utilization will be explained in terms of 1) the research goal, 2) the individual issues and strategies for solutions and the results, and 3) the evaluation of the adequacy of the strategy, in relation to the changes in the changes in the organization of AIST. Finally, the future issues will be discussed[Note 1] (Table 1).

2 Goals of R&D at various periods

2.1 Position of R&D in the whole picture

Recently in Japan, the energy issue in 2100 was discussed in terms of the limited resources and environment, and the direction of the technological development was laid out to deal with the issue[1]. It is estimated that sustainable development will be possible only through thorough energy saving by using electric power that is superior in efficiency, convenience, and economy, and such power is attainable by the massive introduction of renewable energy and nuclear power. Needless to say, power electronics will become important as the common basic technology that will be the key to the effective use of electric power. The key technology of power electronics is power device. While the researchers try to increase performance by improving the design of the structure of the current silicon semiconductor power device, it is approaching the theoretical limit calculated from the physical parameters of silicon. The major performance index of a power device is how low the loss is. To achieve the low-loss property, the low on-resistance (where the resistance during current conducting is low) and high switching speed are required. In the SiC wide-bandgap semiconductor that has a band gap about three times greater than silicon, the dielectric breakdown field is about one digit greater than silicon, and the theoretical limit of the on-resistance is less by two digits. In silicon, a power device with low on-resistance yet with low switching speed (IGBT) has been developed, although its application is limited. The SiC power device that allows low on-resistance and high-speed

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Table 1 Flow of the activities

Organization	Material Science Dept., ETL (1993~2001.3)	Power Electronics Research Center, AIST (2001.4~2008.3)	Energy Semiconductor Electronics Research Laboratory, AIST (2008.4~)
Main activity	· Survey (FY 1994~1995) and leading research (hard electronics) (FY 1996~1997)	· Development of Basic Technology for Ultralow Loss Power Device (FY 1998~2002) · 2 topics in open proposal for energy saving (FY 2003~2005) · 3 topics subcontracted to AIST (module, power supply, system) (FY 2002, 2004, 2003~2006 respectively) · "Development of Basic Technology for Power Electronics Inverter" (FY 2006~2008)	· Industrial Transformation Research Initiative (manufacturing line for SiC device prototype) (FY 2008~2011) · Development of Basic Technology for Future Power Electronics (FY 2009~2012)
Goal	· Clarification of goal →Power device	· Total solution strategy (concurrent development of wafer – device – equipment)	· Concurrent development of demonstration, core, and pioneering researches
Main result	· NEDO project starts	· Construction of SiC basic technology in Japan · Clarification of possibility of SiC power devices and equipment (wafer quality, low-loss and reliability of devices, increased power density of equipment) · Establishment of wafer venture (LLP)	· Demonstration of application to equipment (joint research with industries)
Notes		· Concurrent development of GaN devices · Participation of experienced people from industries · Construction of device fabrication line	· International exchange and collaboration

switching in wide blocking voltage range (MOS-FET and junction FET) will alleviate the limitations of the silicon power device. The power loss during device operation can be reduced by low on-resistance and high-speed switching, and with the downsizing and simplification of the heat dissipation structure (heat release fin or fan) as well as downsizing of the passive components through use of high-frequency, significant cost reduction can be expected for power electronics equipment such as inverters, and this will eventually lead to energy saving. The increased power density (or the downsizing) of the electric power converter is an important index in introducing the converter to society, and has been indicated in the roadmap (Fig. 2). In addition, the high blocking voltage, high-temperature operation, and high breakdown resistance of the SiC power device are expected to allow pioneering new fields of power electronics application. To "achieve the ubiquitous power electronics" that support thorough energy saving, the practical utilization of the SiC device is expected to play an extremely important role.

2.2 Goals during the ETL period (1993~2000)

Material research should not stop at the search in the style of the material science, but should aim for the practical utilization by clarifying the principle superiority through creation of actual devices in a wide sense. The potential of SiC, GaN, and diamond as devices were carefully reviewed, and the research subjects and the goals were narrowed down. The goal was set "to show that SiC possessed principle superiority in the power device application against current silicon in the wide band gap semiconductors, and also to show that SiC has a leading edge compared to other wide

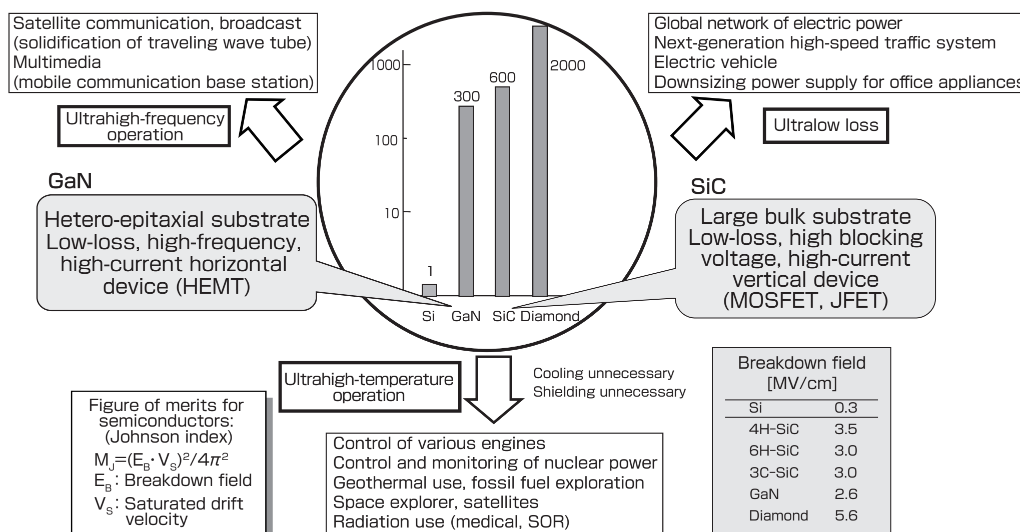


Fig. 1 Hard electronics (the world of wide-bandgap semiconductors)

In the wide bandgap semiconductor, the dielectric breakdown field is large and the saturated mobility rate is also large. Therefore, the figure of merits of the semiconductor is one digit greater compared to the silicon semiconductor devices. The on-loss (current-conducting loss) of the SiC power device is estimated to be 1/200 of the Si device.

band gap semiconductors in practical application".

2.3 Goals during the AIST period (2001~2007)

The ETL was reorganized as AIST, just when ETL was playing its role in the concentrated research for the "Development of Ultralow Loss Power Device Technology" (FY 1998~2002), a project of the New Energy and Industrial Technology Development Organization (NEDO). Through the discussions with the researchers of the power electronics application in the "Next-Generation Power Semiconductor Realization Commission" conducted under the project, we became aware that "although the power device may be the key to power electronics, collaborative development along with the development of converters and system application is mandatory in order to realize the power device". Proposal was made to establish the Power Electronics Research Center (PERC) that engaged in the integrated R&D from material and device development to converter and system application. This was approved. The goal of this research center was "to clarify the contribution to the ubiquitous power electronics (that is the innovation in power electronics) by increasing the performance of the SiC power device and to gain prospect for its system application".

2.4 Goals of the AIST period (2008~)

As the activities at PERC was recognized and the decision was made "to act in unison as a R&D group to take the next step" at AIST, the Energy Semiconductor Electronics Research Laboratory (ESERL) was established to follow PERC in 2008. The next goal was "to continue the integrated effort of wafer and material technology, device technology, and systemization technology, and to generate innovations in power electronics by accelerating the practical utilization and diffusion of the SiC power devices".

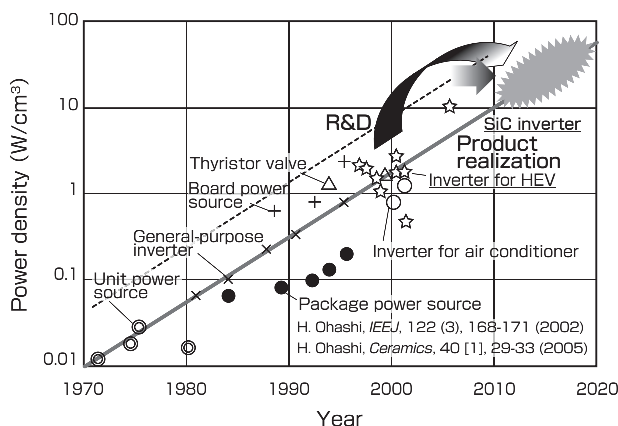


Fig. 2 Roadmap of power converter seen in terms of power density

There has been a double-digit increase in the last 30 years. While the efficiency of the converter is becoming saturated, the increase of power density will lower the cost of the converter, and this will be a major point for the diffusion. The demonstration of R&D sample is necessary 10 years ahead of the product realization (R&D line).

3 Issues extracted, strategies to solve the issues, and the results during each period

3.1 Strategies and results of the ETL period - Construction of the foundation of the SiC power device development in Japan -

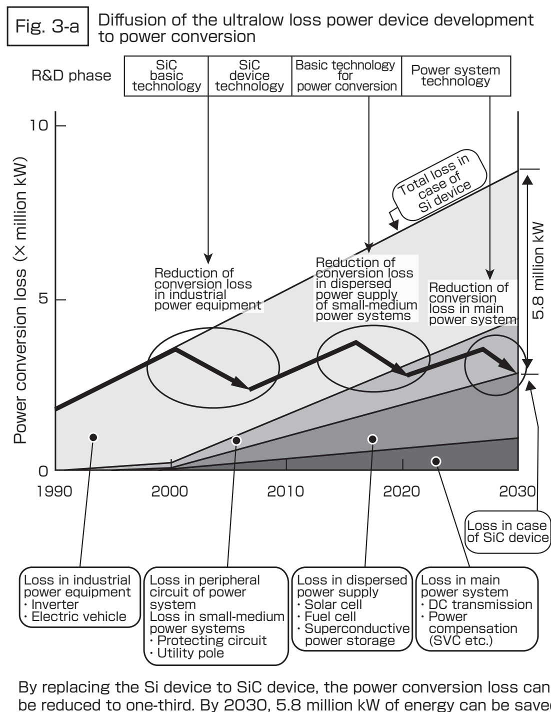
At ETL, a pioneering R&D was conducted where the 3C-SiC (cubic crystal), which was the low-temperature polymorphism of the SiC crystal, was hetero-epitaxially grown on the silicon wafer and the prototype diodes and transistors were fabricated to demonstrate the device property[2]. The SiC device R&D projects supported by the government in the 1980s were started together with the "superlattice device" project and "3D circuit device" project under the "R&D Program on Basic Technologies for Future Industries". However, as the main goal was the environment (heat and radiation) resistant devices (mainly GaAS devices), the industries felt very little attraction and the projects were continued with minor effort. In the beginning of the 1990s, the 30 mm diameter SiC monocrystal (hexagonal crystal) became commercially available in the United States, and the expectations for SiC in the power device began to rise.

3.1.1 Narrowing down to SiC for use in power device and concentrated research method

In the United States, the R&Ds for SiC and diamond as the electronic devices for military application became active under the support of the US Defense Advanced Research Projects Agency (DARPA). In Japan, it was necessary to clarify the positioning of the wide-bandgap semiconductor R&D for the purpose of industrial application. In 1994, the survey of the necessary fields and the available technology was started under the Japan Electronics Industry Development Association (JEIDA). It was proposed that the wide-gap semiconductor SiC, GaN, and diamond would be the semiconductor materials that may enable a device that was resistant to extreme conditions such as high-power, high frequency, and extremely severe environments. It may pioneer a new electronic field called "hard electronics"[3] (Fig. 1). After two years of NEDO leading research "Hard Electronics" (FY 1996~1997), the goal was narrowed down to the development of the basic technology for the low-loss power device that might have great impact on industry, focusing on SiC for which the commercial sale of two-inch wafers was started. The five-year NEDO project "Development of Ultralow Loss Power Device Technology" (FY 1998~2002) was started in 1998 (NEDO and Research and Development Association for Future Electron Devices (FED)). The project was powered not only by the statement, "Although this R&D is conducted for military application in the United States, the basic research that has potential of blooming as an industry should be supported by the Ministry of International Trade and Industry (the present Ministry of Economy Trade and Industry (METI))", but also by emphasizing that a great energy saving can be expected by

introducing the SiC power device, and a new device industry using the SiC semiconductor would rise (Fig. 3).

In the “Development of Ultralow Loss Power Device Technology” project, it was necessary to quickly build the wafer technology and the device process technology that would serve as the foundation of the power device development in Japan, which at the time was mostly basic research. Therefore, the Schottky diode for which practical devices have been developed was not set as the main subject, but the development was narrowed to the basic technology for the switching device that might bring about innovation in power electronics. In this project, the three device manufacturers that were capable of fabricating the FET device -- Hitachi, Ltd., Mitsubishi Electric Corporation, and New Japan Radio Co., Ltd. -- developed the prototypes for different types of FET (MOSFET, JFET, and MESFET) in their laboratories. Concurrently, this was a project in which the integrated basic R&D of material, process, and device was conducted by the industry-government-academia at AIST. This was a concentrated research method where the participating researchers would convene in one place, as a joint R&D with the R&D Association for Future Electronic Devices (Fig. 4). The mixed groups of industry-academia-government were formed for each main elemental technology to engage in the technological development of the SiC semiconductor, since it required different elemental technologies from those for Si semiconductors. This project helped build the foundation of the SiC power device R&D in Japan, along with the NEDO Important Regional Technology Development “Development of Control System Technology for Combustion to Rationalize Energy Use” (FY 1994~1999) that was conducted in the Kansai region for six years from 1994, led by Professor Hiroyuki Matsunami of the Kyoto University (currently director of Campus Plaza Kyoto). In May 2000, an international workshop was held to announce the national SiC R&D to the world[Note 2]. This was effective in obtaining international cooperation in the field where there were very few researchers. The development approaches and results that were unique to this project will be described in the next section.



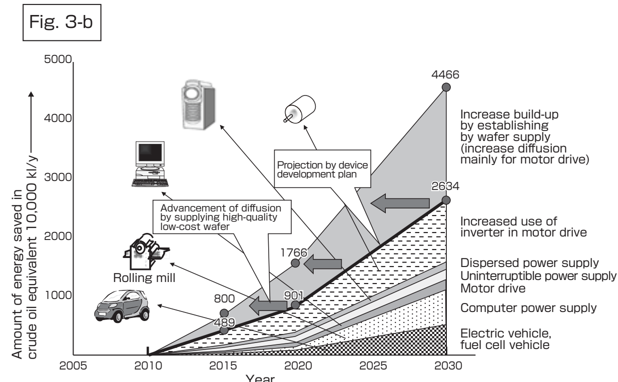


Fig. 3 Effect on energy saving when the SiC device is implemented in Japan

The original figure was published in *Kogyo Gijutsu* (H. Ishii, Aug 1997) (Fig. 3-a). After several revisions, it was used in the *Strategy for Energy Saving Technology* (Fig. 3-b).

3.1.2 Results of the “R&D of Ultralow Loss Power Device Technology” project

At the time, the SiC wafer was supplied almost exclusively by Cree, Inc. of the United States. When a device manufacturer wishes to invest safety in the product realization of a device, it is necessary to have a second source that can provide a stable supply of the wafers. With the exclusivity of supply, there was concern for the stability of the supply, and as the price and the quality of the wafer depended on one company only, the device company will have less say in the wafers that are linked directly to the cost reduction and performance increase of the device. Therefore, under the concentrated

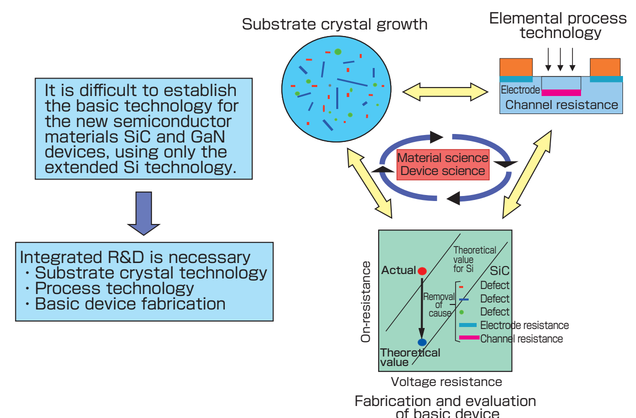


Fig. 4 Development concept of the NEDO project “Development of Basic Technology for Ultralow Loss Power Device”

research method, the project formed a group consisting of ETL and two companies (Showa Denko K.K. and Denso Corporation; later joined by Nippon Steel Corporation) that have started the growth of SiC monocrystals. The approaches selected for this R&D were the on-site observation of x-ray topography of the crystal growth process and the in-furnace visualization by simulation (Fig. 5)[Note 3]. In fabricating the device, a micron-order hole accompanied by screw dislocation in the wafer (micropipe) would be fatal. Therefore, the objectives of the project were the fabrication of a two-inch substrate without micropipes and the growth of crystals with external diameter of four inches. An important technological contribution was the scientific presentation of the crystal growth technology that was a corporate know-how that had not been disclosed until then at academic societies. After the completion of the project, the developed technology was transferred to several Japanese companies that wished to manufacture the crystals.

In high blocking voltage and high-power vertical power device, the low resistance is achieved by introducing impurities at high concentration (the n-type semiconductor is normally achieved by nitrogen doping) to the substrate crystal. Therefore, to realize the desired device characteristics, the homo-epitaxial monocrystal film growth technology is important where the film is formed on the SiC monocrystal by carefully controlling the film thickness and the impurities concentration. The group led by Professor Matsunami of Kyoto University developed a step-controlled epitaxy where high quality growth could be achieved at relatively low temperature (~1600 °C) by introducing the off-angle surface. The project introduced an overseas epitaxial growth system with established performance, and the necessary epitaxial film was supplied to the device fabrication group after fine-tuning the growth conditions. On the other hand, a new high-speed epitaxial device was developed (few years later, this achieved a growth rate of over 100 μm/h on a three-inch substrate). Near the completion of the project, in addition to the silicon face that was the crystal-forming surface of the device thus far, the epitaxial film growth technology that allowed control of the impurities in the carbon face, which is the other side of the silicon face, was developed. It was demonstrated that the channel mobility of the MOSFET was almost one digit greater compared to the silicon face, and the basic device patent was obtained for the carbon face device (Fig. 6). At present, there are still issues that must be resolved in the carbon face device process, but it is developing into a main technology toward practical utilization.

Although the advantage of SiC is that a SiO_2 insulating layer can be formed by thermal oxidation, the channel mobility of the MOSFET obtained by oxidation is extremely low compared to the bulk (in normal thermal oxidation, it is two digits less than the mobility of bulk). The thermal diffusion of impurities that worked extremely well in the silicon process could not be used in the SiC process, and the high-temperature ion injection followed by the high-temperature activation process was necessary. The development of low resistance contact formation technology had to be done quickly. Also, the device parameters necessary for the device design were uncertain or unavailable. These issues were handled systematically in the concentrated research method. For the necessary physical property and process evaluations, we asked the cooperation of universities and external organizations. These results helped build the foundation of this field in Japan that was behind in the device technology development, as well as demonstrated the performance of the prototype SiC power device that surpassed the performance of silicon created by the dispersed research method.

Another important characteristic of this project was that it was conducted under the Engineering Advancement Association of Japan (ENAA), an organization that emphasized the R&D of system application of the practical utilization research (NEDO project “Development of

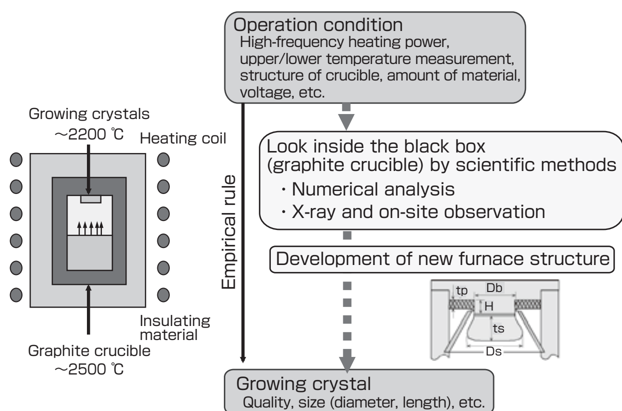


Fig. 5 Approach for the development of SiC monocrystal growth technology
The structure inside the furnace was almost never disclosed at the academic societies or any other places.

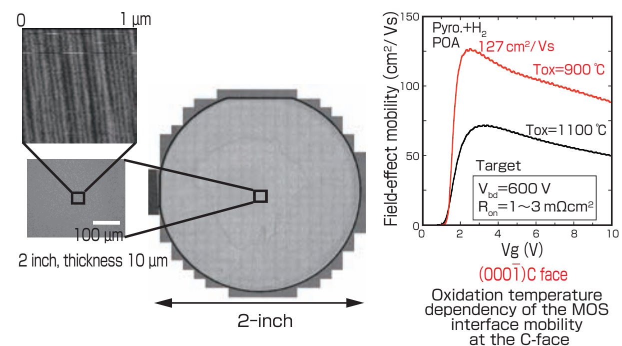


Fig. 6 Development of the carbon-face device technology
The development of the epitaxial growth technology on the carbon face (C-face) and the channel mobility of MOS fabricated on the face (Morphology of the epitaxial surface (the water-like smudges are image artifact)).

Ultralow Loss Power Device Technology: Practical use survey of the future power semiconductor device", FY1998~2002, ENAA). This activity promoted the exchange between the basic research and application fields, and we were able to make prospects that SiC was superior in principle against silicon in the industrial application of the power devices.

To widely spread these results, these results were comprehensively described in a book[4].

3.2 Strategies and results of AIST period (2001~2007) - Proposal of a total solution from wafers to a system -

There were two years left of the NEDO project, and a structural organization from the Agency of Industrial Science and Technology to the National Institute of Advanced Industrial Science and Technology occurred in 2001. In this reorganization, the research centers were designed as units with specific missions. In this R&D phase, we were beginning to see the prospects of the SiC power device. Whether the new device would be practically utilized in power electronics depended not only on the performance of the device, but it was clear that we needed to optimally integrate the various elemental technologies that tended to be at trade-off with each other (Fig. 7). During this period, R&D of power electronics in Japanese industry was difficult due to the reduced investment in infrastructure. For R&D for the practical utilization of the new power semiconductor device, the role of the public institution was important in the long-term R&D. With this thinking, we conducted an integrated basic R&D (total solution) in one research unit that included everything from material and device process development to converter and system application. We declared the realization of "the innovation of power electronics through innovative power device", and established PERC composed of five groups.

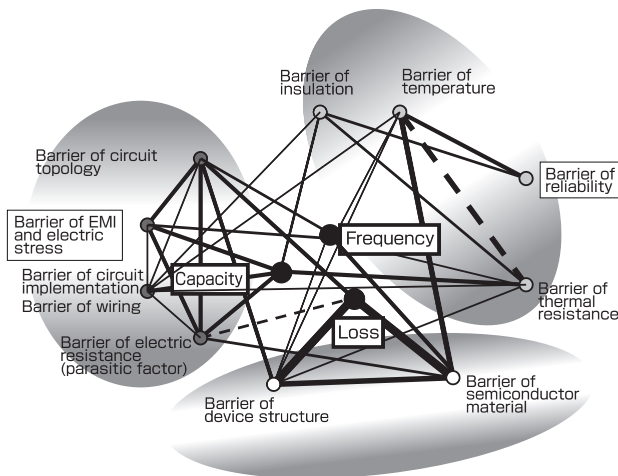


Fig. 7 Various issues of the power module technology

The various elemental issues are complexly interrelated, and must be solved concurrently (created by Ichiro Omura, Toshiba Corporation, Next-Generation Power Semiconductor Device Commission).

During the first half period of PERC, the effort was spent on achieving the goal of the "Ultralow Loss Power Device" project. This was incorporated into the goal of "the innovation of power electronics through innovative power device", and the activities commenced fully. There were 14 full-time staff members, while there was no full-time staff in the Circuit and Implementation Team, and the researchers from other research units in AIST concurrently worked for the Implementation and System Application Teams. At the commencement, from the perspective of selection and concentration, there were questions raised about such an integrated approach. However, it was gradually accepted since one of the central tenets was the promotion of "*Full Research* based on *Type 2 Basic Research*" as declared by AIST. The staff was increased to 18 people in 2007, and combined with the full-time members and the five dual-duty researchers, there were over 80 people involved.

When the "Ultralow Loss Power Device" project was completed, the R&D at AIST was continued as two topics of the NEDO open proposal for Energy Saving (FY 2003~2005), "Basic Research for Ultralow Loss Device, MOS Reliability and High Power Densification of Converter" and "Development of Advanced Diode", jointly proposed with the corporations for further practical utilization. As a result, it continued on to the NEDO project "Basic Technology for the Power Electronics Inverter (or the "Inverter" project)" (FY 2005~2007). There, the demonstration of the converter was conducted with Mitsubishi Electric Corporation. R&Ds for the current capacity increase, high reliability (MOS oxidation film) to warrant the realization of the power device, and R&D to seek potential of high power densification of the converter were conducted with the corporations through the concentrated research method.

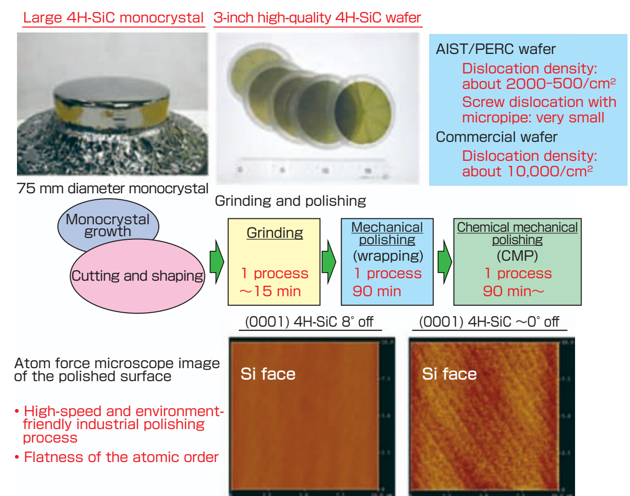


Fig. 8 Fabrication technology of SiC monocrystal wafer

Increasing the quality and decreasing the cost of wafer are the primary issues in the practical utilization of the SiC power device. For decreasing the cost, the development of peripheral technologies such as monocrystal cutting and polishing is also important.

3.2.1 Contribution to the wafer issue

The technologies developed in the project were published at the academic societies, and were actively transferred to industry. Considering the repeated A-face growth (RAF) method developed in Japan, developments were conducted to reduce the crystal defects and to increase the diameter. Also, the cutting and polishing technologies essential for the fabrication of the wafer and the technological transfer were conducted (Fig. 8). In epitaxy, it was found that the growth was possible in the off-less face on the C-face, and the mobility at the MOS interface formed on the C-face was high. To promote the practical use of the epitaxial technology based on these findings, a joint research system was formed by the Central Research Institute of Electric Power Industry, Showa Denko K.K., and AIST. A limited liability partnership (LLP) called the ESICAT Japan, was established based on this research to construct the epitaxial wafer supply system that was the rate-controlling factor of the R&D (that is the controlling factor of the turn around time of device fabrication), and to utilize these wafers in the "Inverter" project. This activity was turned over to Showa Denko in 2007.

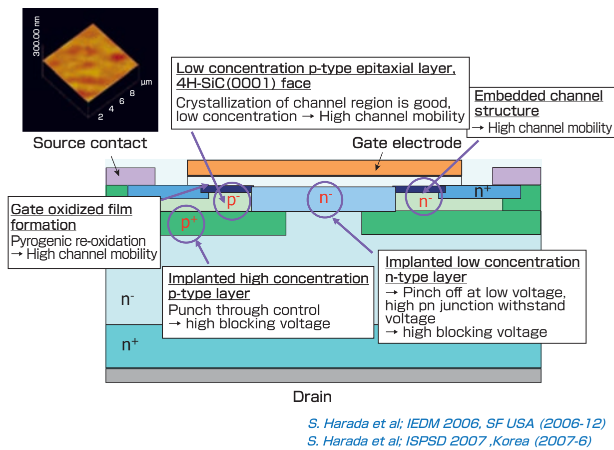


Fig. 9 Device structure of the IEMOSFET (implantation and epitaxial MOSFET) fabricated on the carbon face and its effectiveness

The surface on which the channel is formed is flattened using the epitaxial growth technology and the ion injection technology (AFM image), to improve the channel mobility.

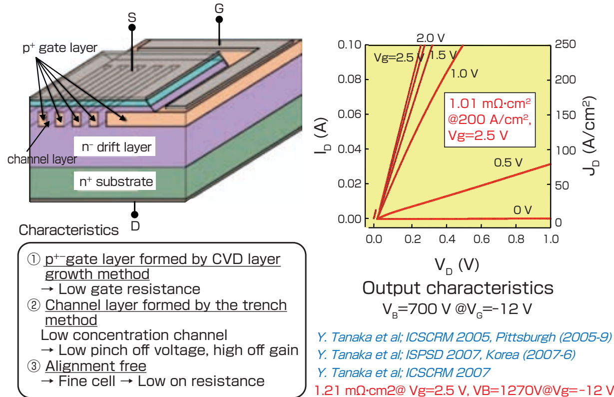


Fig. 10 Structure of buried gate type SIT and its static property

Although it is normally on (it will not turnoff unless gate voltage is applied), the current-conducting loss is extremely low. The epitaxial growth technology also plays an important part in this device.

3.2.2 From principle demonstration of the power device to converter

For the switching device, the development of the junction FET (JFET) was conducted. Although the ampere class device was available on the market, it has not been widely used since it was a normally-on device (a device that is switched on at zero gate voltage). MOSFET has not been marketed since the MOS channel mobility can not be increased and the reliability of the oxidation layer is unclear. AIST developed the Implantation and Epitaxial MOSFET (IEMOS) by utilizing the epitaxial process of MOS channel by employing the high channel mobility of the carbon side, and succeeded in the principle demonstration of a device with world lowest loss. For JFET, using the imbedded gate structure (static induction transistor (SIT)) made by the epitaxial technology, we succeeded in the principle demonstration of low on-resistance to the level where further reduction of the substrate resistance would require further performance improvement (Figs. 9, 10 and 11). The device process technologies became intellectual properties, and were technologically transferred to industry as needed.

For IEMOS, the prototype of the ampere class ultralow loss device was fabricated and supplied in the "Inverter" project.

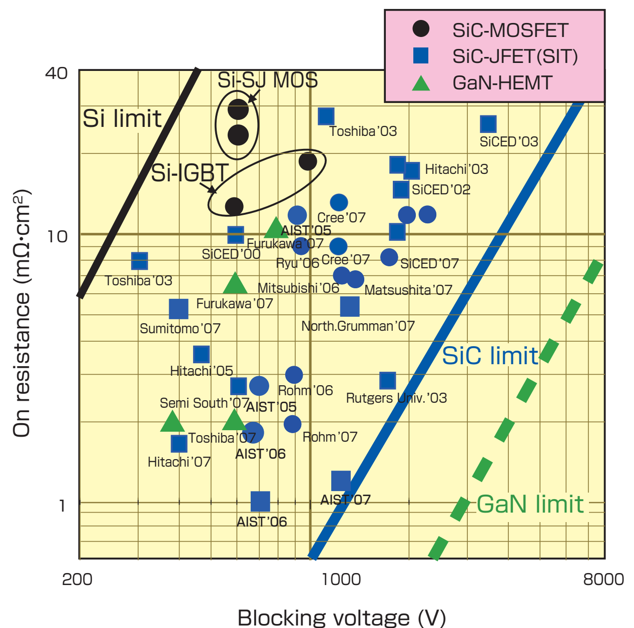


Fig. 11 Trends in the on resistance and blocking voltage of the ampere class switch

AIST has yielded top results in the world. For the recent trends in the Si devices of IGBT and J-MOS as well as the trends of the SiC power devices in the world, refer to "Technological innovation and application of power electronics taken to the next step" by Kazuo Arai in *Ohm* November 2009 issue in Japanese.

By the end of the project, the conditions for realizing the high power density converter of 50 W/cm^3 were clarified. To set the milestone of the technological development at the research center, we utilized the "High-Tech Manufacturing" Research Program established by AIST to promote the manufacturing technology in 2006. There, the crystal substrate, epitaxial film, IEMOS and Schottky barrier diode device, and chopper circuit were fabricated jointly with the three research teams, to achieve the control of the generator motor and to verify the total solution (Fig. 12). For the JFET (SIT) and PIN diodes, there were no concern about the reliability of the gate oxide, and the fabrication technology was developed and obtained a yield that allowed the device to be supplied for the converter. The joint research for system application was started with the corporation around 2007, and the results have been obtained starting in 2008.

3.2.3 Increased current capacity and reliability of the device and the wafer quality

For the demonstration of the power device for its practical utilization, device chips of over 10 A to 100 A were required. At the point of 2005, reports of increased current capacity were starting to be heard for the Schottky barrier diode, while the development was delayed in the switching device. The quality of the wafer (such as crystal defect) was considered to be the major cause. Considering the result of the leading research for energy saving, the "Inverter" project set the goal of clarifying the wafer quality to achieve the high-capacity chip of 100 A class. In reality, the monocrystal substrate had about 10,000 /cm^2 of crystal defects (dislocations). Therefore we worked to clarify the relationship with the crystal defects and the reliability of MOS and increased device capacity that was not studied seriously until then. The crystal defect evaluation using the synchrotron radiation light was deployed at AIST. We obtained the conclusion that while certain degree of reduction in crystal defects was desirable, we could go ahead with the current crystal quality through the advancement of growth technology of the epitaxial film formed on the crystal substrate for fabricating the device (minimization of the surface defect during epitaxial growth, conversion of the crystal defect type, etc.), and work on the device process (gate oxidation layer formation where both channel mobility and reliability are obtained, high-temperature ion implantation and post activation process, etc.).

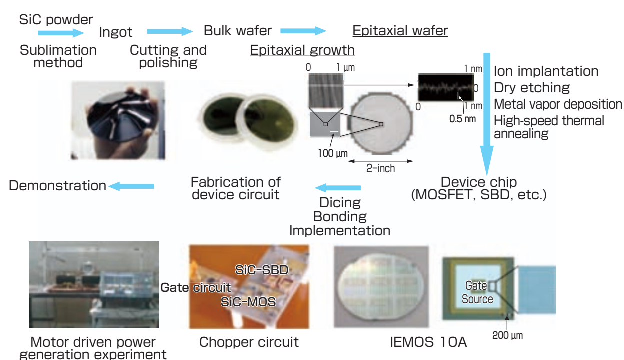


Fig. 12 Demonstration of the total solution by all PERC technology (wafer – device – converter) in the "High-Tech Manufacturing" Project (see text)

3.2.4 Construction of the converter design method and application to high power densification

The conditions and environments in which the power electronics devices are used are varied, and optimizations were obtained by trial-and-error in the past developments. The desired performances of the devices differ according to the use. Particularly, the SiC power device is used for high-speed switching under the condition of high current and high blocking voltage, and the integrated design of device circuit, passive components, and converter structure to maximize the device performance is also important (Fig. 13). For example, at higher frequency, the effects of floating capacitance and floating reactance that did not have to be considered before manifest, and their evaluation and reduction become necessary. AIST developed the circuit integration design composed of device simulation, filter performance, control method, and others, and developed the "simulator for converter loss integrated design" in the "Inverter" project. Combined with the prototype evaluation of the low-loss SiC-MOSFET, we clarified the condition for the high power density of 50 W/cm^3.

3.3 Strategies and results of AIST period (2008~) - Resolving the bottleneck to the practical utilization -

After 2008 at AIST, the wafer, device, and converter that completed the principle demonstration advanced to the downstream demonstration research, and this flow is an important approach for the practical utilization of SiC. During this period, AIST set as its goal the basic research with higher goal needed for the R&D that spiraled upward,

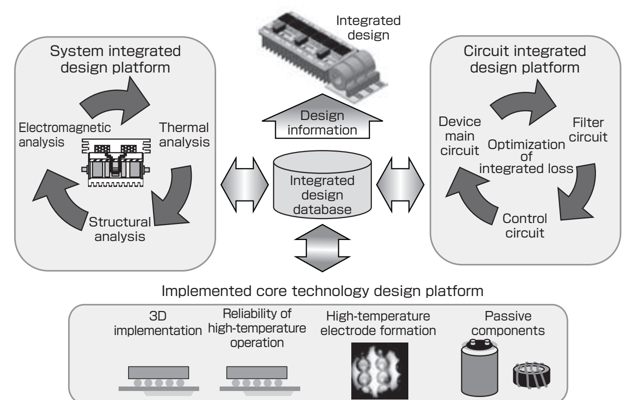


Fig. 13 Conceptual diagram of the integrated design for power converter

The integrated loss of device – filter (magnet) – control is simulated. This will enable optimization of the loss in the circuit design. The integrated loss design simulation of the converter becomes possible by integrating the database of the passive components and the structural factors.

and to engage in pioneering research that may contribute to further developments in this field.

With the demonstration of the 70 % loss reduction for the 14-kVA inverter by a company in the “Inverter” project and the potential for the device application at the current crystal quality through the concentrated research method, the “Basic R&D for Future Power Electronics” (FY 2008~2011) started within the framework of the Green IT project from FY 2008. There, the demonstration of power electronics device with clear application was conducted by Hitachi Ltd. and Mitsubishi Electric Corporation, as well as the basic technology development aiming for the high power density (development of the ultralow loss device and demonstration of the prototype for the high power density converter) through the third concentrated research at AIST.

In the development of the wafer technology, the development of the four-inch wafer was accomplished in Japan in the end of 2007, and this accelerated the practical utilization. In the sublimation crystal, issues remain in increasing the diameter (six inch or more) to reduce the cost of the device, as well as other cost issues such as the productivity of cutting and polishing technologies. The epitaxial technology plays an important role in the formation of the device structure, and the diffusion of high-quality epitaxial technology is also important. Moreover, it is necessary to pursue the new growth technology to replace the sublimation method to increase the crystal quality, and we are starting activities to address those issues.

SiC power electronics was undergoing an evolution in the wafer and device developments, and the interest in its practical utilization was rising. However, for the wafer industry, the demand projection was unclear, and industry was hesitant to make any large-scale investments. For the device industry, the market projection considering the quality and cost of the wafer was unclear, and it was difficult to make a decision for full production. Also, for the companies involved in system application, the device was not readily available. The situation was a so-called “three-party deadlock”. It was necessary to provide support so this relationship would turn into positive feedback for each other. The technological support for the wafer industry, where the expensive epitaxial growth device was the bottleneck for commercialization, came in the form of ESICAT Japan, LLP.

At AIST, the “Industrial Transformation Research Initiative”, the large-scale collaborative project of industry-academia-government, was conducted for several topics. From the end of the FY 2008, the Industrial Transformation Research Initiative “Mass Production of SiC Device Prototype and System Application Demonstration” started its three-year course. Through the collaboration with a device company, Fuji Electric Holdings Co., Ltd., we aim for a practical production technology for the device chip, to quickly supply the device chips to the companies and universities that are attempting system application to the converter, and to clarify the potential of the application field.

4 Evaluation of the strategy

4.1 ETL Period

4.1.1 Narrowing down the development target to SiC power device

Through the exchange with the people in charge of surveys and policymaking, the target of “Hard Electronics” was narrowed down to the SiC semiconductor, where the wafer development was already being done to create the power device. We were able to clarify the vision of creating a new industry and the contribution to energy saving. Through long-term survey, the system for a national project became possible. Flexible responses were made to accommodate industry, and the dispersed research method (involving three companies) for the device development and the concentrated research method that aimed for the construction of basic technology functioned effectively. These were extremely useful for the development of this field later.

4.1.2 Space for the start-up of R&D and procurement of human resources

At ETL, the project started as a group of participants and post docs within the institute mainly among the material and property researchers. In the concentrated research method, the role played by the participants of the companies was large, along with the use of the corporate facilities. The material and property researchers employed as post docs were encouraged to grow into people who could take charge of the device process, and they would eventually engage in prototype production of simple devices. Care was taken in the management, such as holding frequent meetings to raise the morale and research potential. The procurement of space needed for the facility was extremely difficult. If there were appropriate space, we would have moved, but the burden of moving was too great on the staff, and we became painfully aware of the importance of infrastructure in device development. At the beginning of the project, some thought that we could stay at crystal growth and epitaxial growth in the concentrated R&D method. However, effort was spent to fabricate the device prototype under thinking “the essence of the material could only be seen when it is made into a device”. Taking a long view, this was a good decision for the continuation of the R&D.

4.2 AIST period (2001~2007)

4.2.1 Establishment of the research center and proposal of the total solution

Before the waves of free economy changed the Japanese society, the R&D for social infrastructures such as power and communication was led by the electric power company

and telephone company (current Nippon Telegraph and Telephone Corporation), and the private companies joined to participate in research under their abundant research fund. Under such privileged technological development, the obtained technological result may be rather over-spec but still could be used to satisfy the demands in Japan. However, as the management tightened up due to increased free competition, the development intent of the companies dropped due to the limited domestic demand projection and reduction in R&D funds. The contraction and corporate merging of the infrastructure R&D occurred, and the R&D environment deteriorated rapidly for power electronics as a whole as well as for infrastructure R&D. Around the world, global corporations such as Siemens, ABB, GE, and others were spending efforts assuming the developing countries as their clients. With such industrial background, we believed the public research institution must play a critical role.

Since AIST started from material research, the development of wafer and device process was conducted relatively smoothly. However, there were hardly any people who had experience developing the actual device that could be implemented to the converter, and this was only possible by inviting veteran researchers from industry. The presence of such invited researchers was extremely important in executing the total solution, along with the cooperation from the Energy Technology Research Institute, Nanoelectronics Research Institute, and Metrology Institute of Japan within AIST. The demonstration of the basic R&D as a whole in the "High-Tech Manufacturing" Research Program was a symbolic accomplishment of the total solution. The state-of-art joint research with the other research units of AIST through the AIST grant from the Ministry of Economy Trade and Industry (METI) played a major role in the construction of the facilities and the operation ("Development of Ultralow Loss Power Module Technology" (FY 2002~2006), "Development of On-CPU High-Speed High-Capacity Power Technology" (2004~2006), and "Development of Operation and Control Technology for Power Equalization System" (2003~2006)). The pioneering research that was conducted under the "IP Integration" research program, where the obtained patents were integrated, became a power in conducting further R&D for ultrahigh blocking voltage devices.

The prospect for a central research center for Japan for power electronics, a major basic technology for future energy saving centering on the SiC power device development, at AIST was not available until 2008. One of the greatest reasons was the R&D prototype manufacturing line for fabricating and providing the prototype devices to places where application could be expected was not up to a satisfactory level. To realize this, the construction of a device foundry, as well as the participation and collaboration of the researchers in system application who can present the required specification for device performance is mandatory. Since 2008, the potential for the former is beginning to take shape as the Industrial Transformation Research Initiative. We hope for the realization of the latter.

4.2.2 Improvement of device technology in the Open Proposal for Energy Saving

After the first five years of the fundamental development project, the section in charge of the project at METI demanded faster practical utilization, and did not approve the continuation of the basic research by the project. At that time, the SiC power device was taken up as future technology in the "Strategy for Energy Saving Technology"[Note 4]. We also held a symposium where the government discussed the expectation for energy saving by the SiC power device and the user companies discussed the applications, to raise the interest for the practical utilization of SiC[Note 5]. This effort led to five topics of the three-year NEDO open proposal for Energy Saving with the collaboration between the industry and the government. In these three years, the companies were able to demonstrate several ampere (A) class devices, and AIST was able to do a principle demonstration of MOSFET as ultralow loss device. Also, high-performance Schottky barrier diode that can directly lead to the performance demonstration for the converter and PIN diode was developed. These results continued on to the development of the NEDO "Inverter" project.

4.2.3 Establishment of ESICAT Japan, LLP

While it is essential to form the high-quality epitaxial film with controlled impurities concentration for device fabrication, the supply of epitaxial wafer was dominated by Cree, Inc. In FY 2005, with the agreement for joint research support, Showa Denko K.K., a company with experience in epitaxial growth, the Central Research Institute of Electric Power Industry, and AIST got together and a limited liability partnership ESICAT Japan was established. The technological topic was the practical utilization of carbon-face micro off-angle-face epitaxial wafer developed by AIST. The aforementioned "Inverter" project did not include the wafer development, and the development support was done through the information exchange on the correlation between the device performance and the wafer quality, as well as supply from the Japanese wafer manufacturers. Fulfilling the expectation, the supply of high-quality four-inch substrate was started in Japan. In the final stages of the project, by fabricating the four-inch prototype of the Schottky barrier diode, it was demonstrated that the quality of the epitaxial wafer was at a practical level. These activities contributed to creating the supply chain for the epitaxial wafers in Japan.

4.2.4 Coexistence with the GaN R&D

In the activities after 2001, we were occasionally forced to select between SiC and GaN. We stated that it was significant to visualize the innovations in power electronics while constantly comparing the advantages and disadvantages of

the two. In the two NEDO projects for SiC, we included a GaN device topic as a side topic for the sake of comparison with SiC. As of now, it is determined that SiC is suitable for high-capacity devices of kV class, while GaN has great advantages in mobility and is promising as the high-speed switching device in the relatively low blocking voltage horizontal power device of less than kV. The GaN research at AIST supported the project in the form of material research in the concentrated research method, in the project for realizing the GaN high-frequency device for direct application of low-power consumption needed in cell phone stations (NEDO "Development of Nitride Semiconductor Low Power Consumption High-Frequency Device" (FY 2002~2006)). The GaN device went into the device phase slightly later at AIST, and its potential was shown in the development of the low-loss device for AC adapters in the NEDO Open Proposal for Energy Saving. For GaN, the key to its practical utilization is the increased quality of the GaN hetero-substrate on the Si wafer, which is hoped to be a low-cost wafer. After 2008, the research for the state-of-art application of GaN device will continue.

4.2.5 Construction of the device process line

Since the project started from material research and its scale was increased to device, converter, and system, we were always short of human resources, facilities, and equipment, and it was mandatory to obtain them. For the clean room facility (including the major equipment for lithography), we were initially totally dependent on the Nanoelectronics Research Institute, AIST. The procurement of R&D funds for the actual device, circuit, and module in the demonstration of the converter was approaching the limit as a single research unit at AIST. With the concentrated research in the two NEDO projects, active participation to the NEDO open proposals, a grant from METI to AIST to further promote the basic R&D, a grant to install large-scale facilities in the institute, and construction of the new building for nanotechnology research, we obtained the understanding and timely support, and finally were able to construct a manufacturing line for the two-inch prototype device. The two-inch line was improved as a place of R&D with industry, and collaboration with companies progressed through the sharing of the know-hows and transfer of intellectual property. In addition, the ultralow loss SIT and PIN diode mentioned earlier could now be fabricated at good yield. Through the joint research with companies, the developments are being conducted for the breaker for DC distribution system (NTT Facilities, Inc. etc.) and the high-capacity converter (Toshiba Mitsubishi-Electric Industrial Systems Corporation, etc.).

4.2.6 Training, international exchange, and collaboration of human resources

In human resource training, the researchers who were capable of thinking and projecting the downstream of their technology were nurtured through the seven-year experience at the research centers of AIST. We have dispatched people to industry. Contribution to the academia includes the activities in the SiC and Related Wide Bandgap Semiconductor Research Group of the Japan Society of Applied Physics and two active participations in the International Conference on Silicon Carbide and Related Materials (ICSCRM)[Note 6]. International collaborations included the activities at the Power Electronics New Wave (PENW) workshop[Note 7]. Through the exchanges at international conferences, we learned that people shared the common consciousness "while power electronics is important, it is an underlying support of society for which the social awareness is low". Information was exchanged among the people who shared the same thoughts at the Center for Power Electronics System (CPES) of the United States, European Center for Power Electronics (ECPE), and AIST. The PENW was held to create a common roadmap for power electronics. The footholds in international collaboration were created through these activities. When the Obama Administration started in 2009 in the United States, environment and energy were listed as important topics, and the R&D in this field is being strengthened. As the follower of CPES, a center for constructing a next-generation microgrid that incorporates renewable energy was established under the support of the National Science Foundation (NSF)[5]. The global competition and collaboration for grid standardization will become an important topic. We believe a quick action based on international perspective is necessary for Japan.

4.3 Industrial Transformation Research Initiative activities at AIST

The SiC Schottky barrier diode has become commercially available. Since it has the advantage of requiring small recovery current when switching, 30~40 % reduction of loss can be achieved by simply installing the SiC Schottky barrier diode as the free wheeling diode in combination with the Si-IGBT device. Therefore, it is almost certain it will be used in diodes. As the market scale of the SiC device is becoming visible, we are now out of the three-party deadlock and are receiving positive feedbacks from various fields. The topic of the Industrial Transformation Research Initiative at AIST is a timely decision to acquire the related intellectual property for the converter application which was lagging behind because we had no supply of the device chip. The main required specifications for the device are different according to the application (Fig. 14).

It is important to consider the changes in the system and the new systems, and not just the advantages of the system from the advantages of the new converter. To do so, it is necessary for the company people to experience using the actual SiC device, as well as the exchange of opinions with various application development fields, in an actual place of joint work where the inadequacies can be pointed out. It is necessary to conduct a LINUX-style development where the

source code of the basic software is disclosed and further developments are solicited from the users. This is a giant step in the *Full Research* for the practical utilization of the new semiconductor device. It can be positioned as the work of constructing the infrastructure in developing the future energy saving system. In quickly executing such large-scale R&D topics, the role of the Industrial Technology Architect (an AIST terminology) who conducts the integration of the funds, facilities, and joint research contracts is crucial. The device evolves as it accepts the required specifications from the system. We are at a phase where the people who bridge the device and system application play extremely important roles. AIST is expected to play the role as an integrator.

5 Future issues

The new government of Japan that came to power in September 2009 is calling to the world for “25 % reduction of greenhouse gases by 2020 compared to 1990”. In the Tsukuba region, there is a plan for the formation of the nanotechno innovation center, in the style of the Interuniversity Microelectronics Centre (IMEC) of Europe and the industry-academia collaborative research in Albany, USA. Power electronics is one of the topics. The clarification of the potential and promotion of further SiC basic research was selected as one of the 30 topics of the “Funding Program for World-Leading Innovative R&D on Science and Technology” of Japan. The R&D for the practical utilization of new semiconductors does not develop sequentially like “wafer → device → system application”. The individual R&Ds progress in a spiral form, for example, in response to “a larger wafer diameter is required” or “higher quality is demanded” with the advancement of device development. We expect that the industry-academia-government will join together to engage in the pioneering basic R&D to ensure practical utilization. We need an integrated R&D that looks at the future of power electronics as the key technology that supports the transformation of the energy infrastructure.

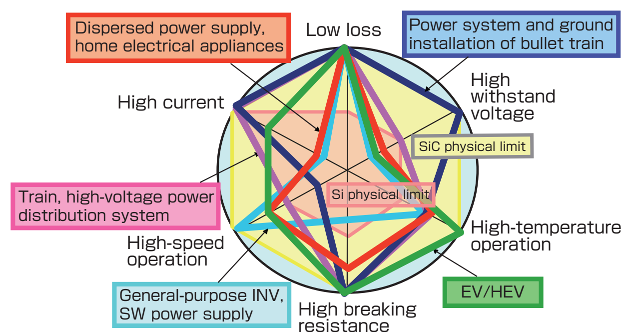


Fig. 14 Conceptual diagram of the application and required device performance
Some of the device performances are in trade-off relationships (for example, low loss – high breaking resistance – high-speed operation). The optimization (tuning) of the device performance according to application is important.

Acknowledgements

I thank Professor Sadafumi Yoshida, Saitama University (currently visiting researcher at AIST) for his judicious advice on this paper. He is the pioneer of the R&D for SiC material and device and has supported our efforts from the beginning.

Notes

Note 1) The structure of the paper was arranged according to the instructions provided by the reviewers, considering the objective of this journal. Therefore, the periods during which certain organizations were active and the periods of the projects do not necessarily match.

Note 2) 1st International Workshop on Ultra-Low-Loss Power Device Technology (UPD2000), May31~June 2, 2000, Nara, Japan (organized by the Research and Development Association for Future Electronic Device).

Note 3) The group led by Professor Madar of the Centre National de la Recherche Scientifique (CNRS), Grenoble, France cooperated in this simulation.

Note 4) The importance of energy saving in the power electronics application was indicated in the “Strategy for Energy Saving Technology” (Energy Technology Policy Division, Agency for Natural Resources and Energy, June 12, 2002). In the revised edition, SiC is acknowledged as the energy-saving device technology for power electronics.

Note 5) Special Symposium “New Start of Energy Saving Technology Development ~ New Developments in Power Electronics”, held on November 25, 2002, at the Zenkyoren Building, Tokyo. Organized by the Information Technology Research Institute, AIST.

Note 6) “Research Session on SiC and Related Wide-Gap Semiconductor”, Japan Society of Applied Physics; International Conference for Silicon Carbide and Related Materials (ICSCRM01, Tsukuba); ICSCRM07 (Ohtsu).

Note 7) 1st Power Electronic New Wave (PENW) International Workshop, held at Hatsumei Kaikan, Tokyo, on April 11, 2005, organized by AIST, supported by FED. 2nd PENW, on June 15, 2006, organized by PERC, supported by FED. 3rd PENW, on January 2008, AIST.
European Center for Power Electronics (ECPE), Germany: an industry-academia-government collaborative effort led by Siemens AG. Established in 2003.
Center for Power Electronics System (CPES), USA: one of the NSF-supported engineering centers composed of five universities and over 80 companies, led by the Virginia Polytechnic Institute and State University. Established in 1998.

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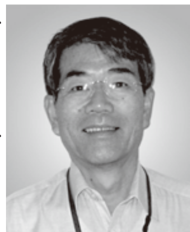
Author

Kazuo Arai



Graduated from the Department of Applied Physics, Graduate School of Engineering, The University of Tokyo in March 1966. Joined the Electrotechnical Laboratory, Ministry of International Trade and Industry in April 1969. Head of the Material Science Division, ETL from January 1993 to March 2001. Leader of the “R&D for Ultralow-Loss Power Device” project from October 1998 to March 2003. Director of the Power Electronics Research Center, AIST from April 2001 to March 2008. Engaged in the R&D from the material and process development of the ultralow-loss power device to the system application of the device. Leader of the NEDO “Development of Core Technology for Power Electronics Inverter” project from July 2006 to March 2009. Currently, visiting researcher of Research and Innovation Promotion Headquarters, AIST. Doctor of Engineering.

Discussions with Reviewers

1 Overall structure

Comment (Yoshiro Owadano, Environment and Energy, AIST)

The first draft is written chronologically, and the social situations, ways of thinking, events leading up to the research, and the results are presented as a mix. Therefore, it is interesting as an article, but it is difficult to follow the logical development as a paper. To contribute to the future discussion with some generalization as “synthesiology”, why don’t you rearrange the structure as follows: 1) research objective, 2) setting of the individual issues, 3) strategy for solving the issues, 4) execution and results, 5) evaluation of the strategy, and 6) future issues and strategy?

Comment (Hiroshi Tateishi, New Energy and Industrial Technology Development Organization)

The first draft is a chronology and commentary of the SiC device development of the past 20 years. Please revise the structure and reconsider the logical development so it will be more suitable as a research paper of synthesiology.

Answer (Kazuo Arai)

I revised the draft as instructed, although there may be some overlaps.

2 Clarification of the research strategy

Comment (Yoshiro Owadano)

The “Innovation of power electronics” in the first draft contains important points, and I think it should be discussed in the beginning. In that case, please organize and discuss whether you intended to replace the silicon with SiC, or whether you intended to replace the mechanical breaker and relay that are fairly functional as they are at the moment, and what would be the advantages of such replacements.

Answer (Kazuo Arai)

I may be unable to discuss too deeply, but I indicated the possibilities and the points of the development. If the cost approaches silicon and the reliability is established, I am certain that the kV or over power devices will become SiC.

3 Reasons for selecting power electronics and SiC

Comment (Yoshiro Owadano)

While it may be true that increasing the percentage (electrification ratio) of using energy as electric power is important, I think you should be aware that is not directly linked to the diffusion of power electronics. Please indicate the uses in which the device must be a power electronics device, specifically a SiC device, and how it is expected to become diffused.

Answer (Kazuo Arai)

The fact that it is not directly linked is the problem, and I think that’s because there are problems and concerns about the cost and reliability of power electronics. Innovations must be done to remove such concerns, and while the SiC device has the potential, there are still many issues that must be solved. I think the strategy for practical utilization is how to overcome the issues considering the external conditions.

4 Reasons for selecting SiC

Comment (Hiroshi Tateishi)

I think you should provide a simple explanation on why you selected SiC as your starting point or the central target among wide-gap semiconductors. It may be obvious to the researcher in charge, but it is the first question for a non-expert.

Answer (Kazuo Arai)

I added the explanation at the beginning of section 3.1.1. The selection of SiC was the starting point.

5 Changes in research strategy

Comment (Hiroshi Tateishi)

I suppose you did not necessarily have a clear long-term strategy from the beginning, but the specs and the strategy evolved as you looked at the relationships between material, practical material, device and system as the research progressed.

Answer (Kazuo Arai)

This was an important point in 2001. I added the explanation in the beginning of subchapter 3.2.

6 Content of “total solution” and “power electronics innovation”

Comment (Yoshiro Owadano)

The original meaning of the phrase “total solution” is to take measures by integrating various methods to solve a major issue. I don’t think its meaning is the same as “integrated research”. Please state the issues that must be solved and clarify the meaning of the term “power electronics innovation”.

Answer (Kazuo Arai)

1) “Total solution” is used in the sense that various methods are integrated to solve a certain major issue. The major issue that must be solved for the practical use of the new semiconductor was the “solution of the three-party deadlock”. To do so, the linear R&D model of “wafer → device → application development” was insufficient, and it was necessary to deal with the issue from three directions (methods).

2) The “power electronics innovation” is a development of “[low loss + high frequency] → low cost converter → ubiquitous power electronics device”.

7 Content of “integrated research”

Comment (Yoshiro Owadano)

In “integrated research”, I’m sure there were shift of emphasis as time went by, allotment of limited resources, and walls between different topics. It will be very useful if you describe how you dealt with those issues.

Answer (Kazuo Arai)

Since this study started from almost zero, we recklessly engaged in whatever we thought was necessary, and were always hungry. If we could not fabricate the device on our own, we could not see any prospect. Therefore, funds were invested in the expensive equipment and facilities for the device process. I added the description of this situation.