Development of diamond-based power devices

— Verification of its superiority as the ultimate power device —

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Diamond is expected to be an excellent material exceeding SiC for producing low loss power devices because of its superior material characteristics. We have developed series of elemental technologies including killer-defect free epitaxial growth, refractory Schottky contact, Schottky barrier height control associated with low leakage current and termination structure. As a result, we have developed a refractory Schottky barrier diode with fast switching capability, which can operate for over 300,000 hours at 250 °C. R&D of large scale wafers and large power devices are required to realize low-loss devices with a new concept of “cooling system free.”

Keywords **:** Diamond, power switching device, refractory, low loss, Schottky diode

1 Objective of the research and its outcome

Diamond is a material with the highest performance among all materials in terms of heat conductivity and electrical breakdown field. It can be called the “super material.” Although there are several applications for diamond, it is best known as the material for wide-gap semiconductors. For power semiconductor devices, its expectation as low-loss power conversion device surpassing SiC is high.[1]-[4] The related material parameters are shown in Fig. 1. The thermal conductivity is one order higher than Si, overwhelmingly higher than AlN, Cu, Al and other heat spreader materials commonly used. It can be easily inferred that diamond may alter the fundamental thermal management of a device. The electrical breakdown field is one order higher compared to other materials, and high breakdown voltage is expected. The high hole mobility is advantageous for high-speed and high-output operations. Also, with increased carrier at self-heating temperatures of 200~250 °C, there is no decrease in output at high temperature, and this property can be used to create an innovative device module without a cooling system unit. Figure 2 shows the correlation between the on-resistance and the breakdown voltage of the Schottky diode at room temperature and at 250 °C. For the property of SiC, the incremental effect of the drift layer[Term 2] due to temperature increase was applied to the optimal structure at room temperature.[5] In diamond, the increase in carrier due to temperature increase supplements the decrease in mobility due to scattering. The current increases to about 200 °C and becomes low on-resistance, and become constant to about 250 °C. Therefore, in case of the diamond, low-loss, high-current, high-voltage, and ultra downscaling are realizable as long as the device that has reached high temperature due to self-heating is not “cooled on purpose.”[6] This property can be applied to power devices such as electrical vehicles, trains, and vessels, as well as industrial devices and for power distribution. Compared to SiC, the CO_2 reduction of 2.34 million ton/year (2040) and 4.93 million ton/year (2050) can be expected. It is mentioned as one of the ultimate devices that may support power electronics in the Cool Earth Innovative Energy Technology Plan[Note)] of the Japan Ministry of Economics, Trade and Industry.

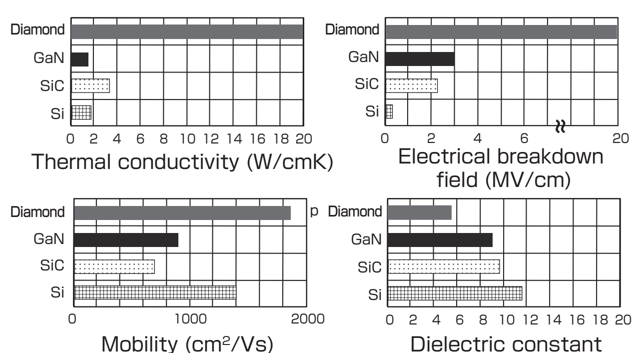

Fig. 1 Comparison of parameters of various materials that affect the power device
(Mobility for diamond is p type)

Because it is composed entirely of carbon, diamond has a major advantage that there is no natural resource problem such as raw material procurement and remaining reserves. It is also highly safe, as it can be synthesized using safe gases such as methane and CO_2, is extremely stable all the way to high temperature, and does not emit harmful substances upon combustion, and is safe at nano size.

In conducting the fundamental researches and various application researches for diamond, in February 2005, we

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started for the first time in the world on the research of its use in wafers and devices for application in power devices. For wafers, there is a report on part of the developmental process (direct wafer technology where the single crystals are fabricated as if being copied, and the realization of crystals with 12 mm sides).[7] This was followed by the achievement of mosaic crystal,[8] and recently the 20×40 mm^2 dimension has been achieved.[9] In this paper, we report Phase 1 of an R&D where the superiority of diamond was verified from the vantage point of devices, taking the example of the Schottky barrier diode (SBD).

2 Research scenario

To realize diamond as a next-generation power semiconductor device, there are, of course, various issues in each phase. The following points must be verified to establish superiority over other materials in Phase 1 (superiority verification).

1) High breakdown voltage (verification of property that surpasses other materials)
2) Operation in high current (density) (verification that high output can be achieved in high temperature)
3) Operation in high temperature (verification of property that enables new concept)
4) Verification of high-speed switching operation

Among the above points, 1) and 3) can be verified using the pseudo vertical device (to match the explanation in the figure) where the process can be carried out relatively easily, but for 2) and 4), a vertical structure[Term 3] that enables practical use is necessary.

The above points were summarized from the perspective of synthesiology in Fig. 3. These are like the combination of the aufheben and breakthrough types that are basic synthesis methods,[10] and it can be concluded that the accumulation of elemental technologies and the breakthrough that enables that are necessary. Figure 4 supplements the explanation of the pseudo vertical and vertical devices shown in Fig. 3. In this synthesis diagram, the low-defect epitaxial growth in the active layer of device (elimination of killer defect in Phase 1) and the heat resistant Schottky formation for high-temperature operation are considered very difficult issues. As shown in Fig. 5, there are defects present due to abnormal growth of diamond in the epitaxial film. In this example, the defects in the growth hillock appear as holes, and these are "killer defects" that are fatal to device operation. This was determined since we detected what seemed like a superimposition of the ohmic flow-through current when we conducted property assessment after fabricating the diode. By studying the relationship between the device yield and the surface area, it was shown quantitatively that such defects directly affect the device yield as shown in Fig. 6. In the example of this epi film, the defect density reached 10^5 defect/cm^2.

3 Example of the elemental technology development

In this paper, the items that were breakthroughs for solving the issues of fundamental technology of the devices will be outlined.

1) Elimination of killer defects

First, pertaining to the low-defect epitaxial film growth in the drift layer that is the active layer of the device, it is widely known that low defect can be obtained by step flow growth in the normal semiconductor material. Since the diamond has bond energy three times the strength of SiC, arbitrary polishing was difficult, creating reproducible steps on the crystal surface was difficult, and experiments could not be carried out easily. Therefore, we conducted the R&D of polishing technology for obtaining a flat surface in arbitrary direction on the diamond crystal and then forming steps. It became clear that this was totally impossible with the

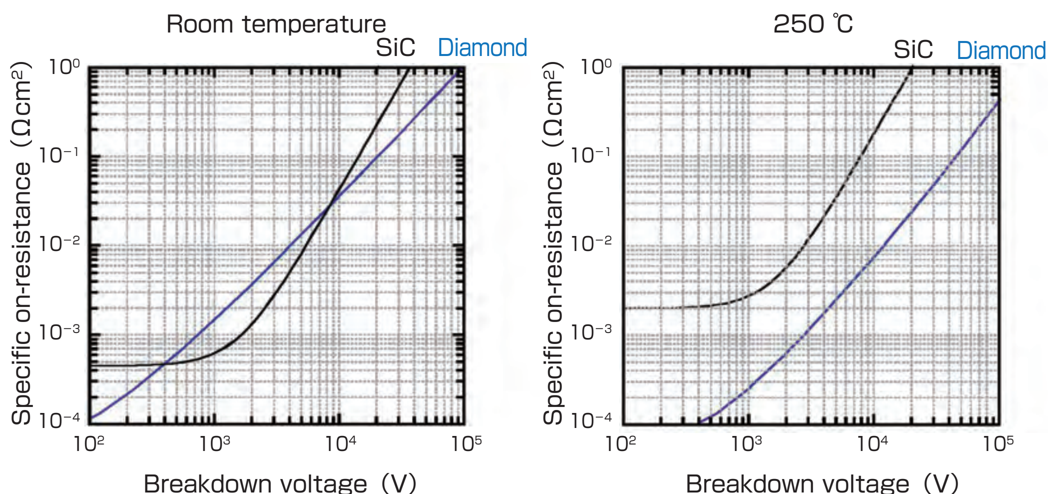


Fig. 2 Comparison of the relationship of on-resistance and breakdown voltage at room temperature and 250 °C

conventional polishing technology. We decided to take this to the basics, and started from the design and fabrication of the polishing device. The two points of the polishing device development were as follows.

(1) An x-ray Laue goniometer was mounted on the polishing head to measure the off angle and off direction by x-ray analysis, to enable polishing in any arbitrary direction.
(2) A weight was placed on the high-rigidity arm for weight adjustment, and the lap was designed with a low vibration structure.

By developing the polishing plate and polishing process as well as the polishing device, we were able to achieve step formation after applying ultra flat processing (arithmetical mean roughness of Ra < 1 nm) on substrates with various off angles and off directions. Using such formations, we investigated the epitaxial layer growth. The epitaxial layer was formed using the CH_4 and H_2 gases with trimethylboron (TMB) as B dopant gas, using the 2.45 GHz microwave chemical vapor deposition (CVD) that is employed normally. While the details will be abbreviated, it was found that in the microwave CVD growth using low density plasma, the abnormal particle defects did not decrease even by changing the off angles and off directions, step flow did not occur well, and there were some variations depending on plasma density. Therefore, we remodeled the CVD equipment to use high-powered plasma. The dependence of the off direction was studied by increasing the power of microwave from 0.75 kW to 4 kW.

As a result, it was found that a giant growth hillock tended to form between <110> and <100>. There were no such hillocks at directions <110> and <100>, nor were there abnormal particles, and an extremely flat surface could be obtained at 2 degrees or more, without dependence on the off angle.[11] Particularly for direction <110>, it was easily estimated that the step flow growth was readily formed since the carbon atoms on the surface formed the dimer row. Figure 7 shows the dependence of the defect formed by the epitaxial growth and the off angles. The situation obtained when the plasma density was changed is also shown. Hence, we succeeded in reducing the killer defect of 10^5 cm^{-2} to almost zero.[11] The flatness Ra obtained by measuring the epitaxial film by AFM was 1.1 nm. When the mobility of the holes in the diamond was measured by hole effect measurement, it was high at 1540 cm^2/Vs, and it was found to be a high quality film. The rate of epitaxial growth in this session (4 kW) was high

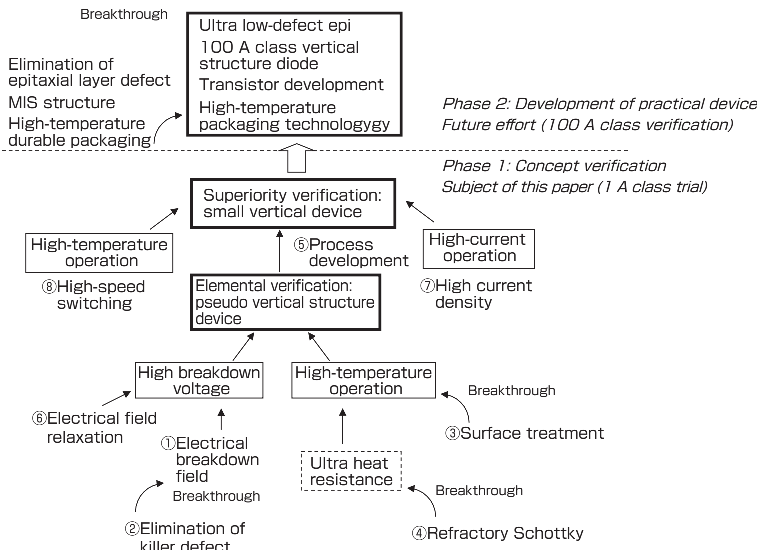


Fig. 3 Synthesiology tree diagram for the superiority verification of the diamond power device
(Numerals are the order of researches conducted)

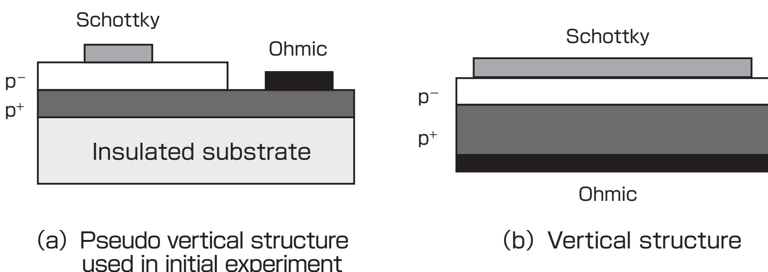


Fig. 4 Structural diagram of the device

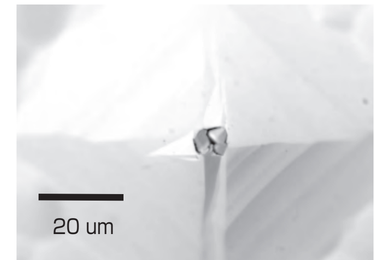


Fig. 5 Killer defect present in the epi layer of diamond

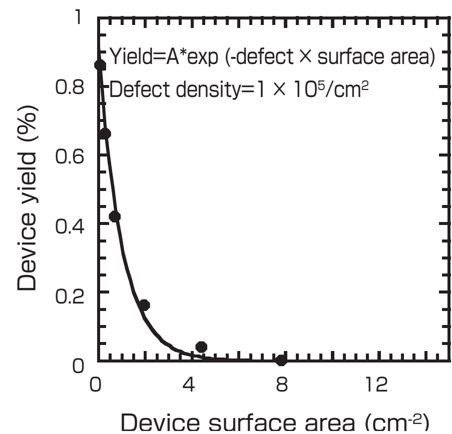


Fig. 6 Relationship between the defect in device and its yield

from 0.8 to 3 μm/hr, or over five times, compared to the 0.2 μm/hr or less of the conventional plasma density (750 W). To maintain the breakdown voltage of the power device, a thick drift layer is necessary as the active layer, so the drift layer epitaxial growth of 10 μm/hr or more is required. In diamond, since the electrical breakdown field is high and only one order less thickness is necessary compared to Si, the epitaxial growth rate obtained in this research is thought to be sufficient for practical application.

As described above, the technology for flat-polishing the wafer to obtain arbitrary crystal off angle and off direction was established, and this enabled nano step control as well as epitaxial growth without killer defects. Prior to the researches of devices and crystal epitaxial growth, we were able to develop the technology by returning all the way to the polishing technology. Thus, we pursued the *Full Research* that involved basic research to application.

2) Schottky interface formation to enable high-temperature operation

Even the mechanism of the reverse-biased leakage of Schottoky interface was unknown in 2005, and we had to start from basic research. To simplify the process, the investigation at this stage was conducted using the pseudo vertical strucutre[Term 3] shown in Fig. 3.[12] The diamond Schottky barrier diode (SBD) was fabricated and the temperature dependence of the reverse leakage current was analyzed. The leakage current increased with the increase in temperature. For example it increased from 10 μA/cm^2 (@2 MV/cm) at 23 °C, to 10 mA/cm^2 at 120 °C. Such figures for the current density level were several digits less than the leakage current observed for SiC SBD in the same electric field. It is difficult to analyze this leakage current according to the model of decreased barrier induced by electric field that is used generally to understand the reverse-biased leakage in Si SBC and GaAs SBD. It was found that the behavior of current voltage property could be explained mostly by using the TFE model[Term 4] taking into consideration the tunnel process by the application high electric field.[13][14] It was necessary to increase the barrier height because the device operation limit was reached by the thermal heat emission current, before the operation limitation due to current amplification led by the avalanche breakdown.[Term 5] Of course, the operating voltage increases if the barrier height is raised, but this was not a problem assuming the high-temperature operation in this case. Therefore, we attempted the method of introducing the localized level for pinning the Fermi level, by applying surface treatment to the Schottky interface. In considering the dry treatment of the diamond surface, we found a way to maintain the high barrier height by introducing the localized level stably through the UV/O_3 treatment.[15] We were also able to observe the reverse field that reached 3.1 MV/cm. Although this localized level has not been identified, we decided to utilize it for engineering purposes. When the Schottky diode was fabricated using this method, the reverse leakage current three order less compared to SiC at high temperature,[16] good forward-biased properties (forward voltage that does not decrease too much at high temperature and low on-resistance due to increased carrier) were observed[17] (Fig. 8).

3) Refractory metal

The next explanation is the breakthrough in the search of heat refractory Schottky electrode. At the time, the heat resistant ohmic junction was already developed, and it was known that TiAu materials including TiPtAu and TiMoAu presented extremely high heat resistance.[18] The difficulty was the Schottky junction. The hurdle was high for the simultaneous achievement of Schottky property, low resistance, adhesiveness, simple process (wafer process and wire bond), as well as heat resistance, and the feasibility of the research was unknown. Investigations were done from both aspects of materials that formed carbide by reacting with diamond at high temperature and those that do not form carbides, but the most prospective stable carbide WC had high resistance and sufficiently high heat resistance could not be obtained.[19] Therefore, we shifted the focus to non carbide forming metals with high melting points. Various metals were tested, and Mo was found to have

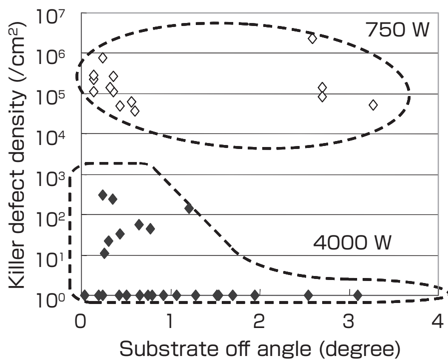


Fig. 7 Dependence of killer defect, substrate off angle, and plasma density

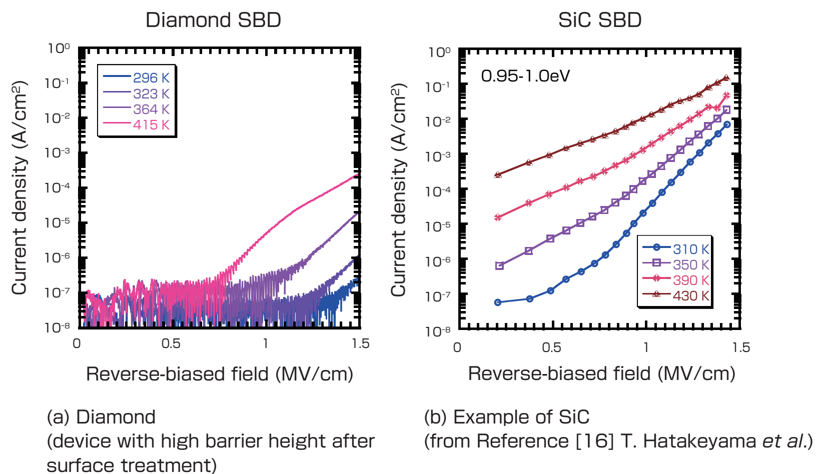


Fig. 8 Reverse leakage current of the Schottky junctio

excellent properties in various items. The development was continued with Mo as the prime candidate. However, when studying the deterioration in high temperature using various devices, it was found that although excellent property was observed in the Schottky junction that was formed in the no-defect area of the epitaxial layer, the reverse leakage current increased depending on the annealing time in the defective epi layer region. This is shown in Fig. 9. The defective area of epi layer had lost the sp^3 bond state, and the carbide was formed as γMoC_{1-x}. Since the reverse leakage current increased in the epi defect region with increased high temperature time, it could not be used practically. Amidst such situation, a young post-doctorate researcher suggested Ru that was successfully used in some previous research in which he was involved, and a test was done by borrowing a sputtering equipment from a different section. As a result, it was found that the above five properties, from heat resistance to ease of processing, were simultaneously satisfied using this metal. In the accelerated deterioration test, there were no changes over 1500 hours at 400 °C as shown in Figure 10, regardless of the presence or absence of defects.[20] It was estimated that ultra high thermal resistance of over 300 thousand hours at 250 °C should be obtained when the activated energy of deterioration by surface graphitization was assumed to be 1 eV. The search for such heat resistant Schottky metal was far from the originally planned R&D. However, by conducting the high-temperature deterioration test at an early stage, we were able to overcome the issue early so it would not be a major problem after the development had progressed for some time. It is also the reality of R&D that progress occurs on a whim as in the Ru suggestion. I mentioned this incidence because I feel that it is very important to maintain some degree of freedom in conducting the R&D.

4 Technological syntheses that were verified

The developments of breakthroughs were explained, among the several research process of using diamond as power devices. For the verification for diamond advantage, various properties were demonstrated using the pseudo vertical structure as shown in Fig. 3. After the development of the process, device, and implementation technology, the operating properties were investigated using the vertical structure, and the following overall superiority of diamond was demonstrated. Although the details will be abbreviated due to space limitations, the properties can be divided in to the following categories.

(1) Electrical breakdown field: verified 3.5 MV/cm with Schottky junction, way surpassing SiC[21]
(2) Elimination of killer defects by improving the epitaxial growth of the drift layer (described in this paper)
(3) Achievement of low leakage current by surface treatment technology and high ϕ_B (described in this paper)
(4) Achievement of ultra high thermal resistant Schottky junction (described in this paper)
(5) Development of vertical device process[22]
(6) Development of field termination structure[23]-[25]
(7) Verification of high current density at high temperature (5 KA/cm^2 @250 °C using small pseudo vertical device)[26]

Additional tests other than mentioned above included observations of property unique to diamonds, such as observing that no hotspots would be formed in diamond through temperature mapping of the device in operation.[27]

The diamond diode that could achieve both high temperature operation at 250 °C and high current density was developed, and this opened the possibility for a power device that does not require cooling, as well as with low loss at high temperature and high breakdown voltage. This is a concept where the device that reaches high temperature through self-heating does not have to be cooled by a large cooling module using energy, but instead, heat is utilized as is.

A prototype of a vertical structure diode was fabricated using

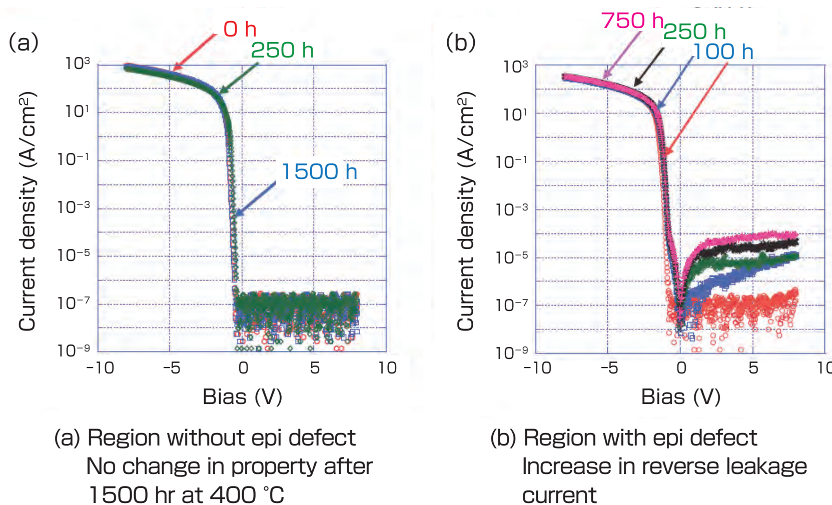


Fig. 9 Property of Mo Schottky junction maintained at high temperature
(From Reference [20] K. Idea *et al.*)

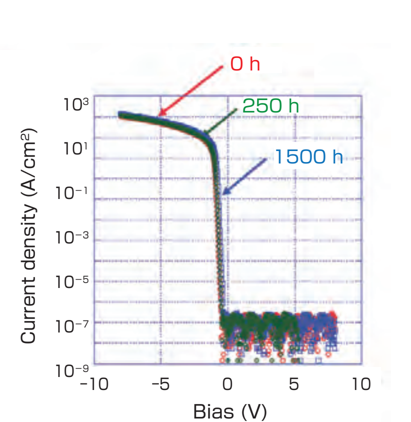


Fig. 10 Property of Ru Schottky junction maintained at high temperature
(From Reference [20] K. Idea *et al.*)

the Al_2O_3 insulating film as the field relaxing structure. As shown in Fig. 11(a), this is a structure in which the Al_2O_3 was set around the Schottky electrode. The prototype of the first ampere class device is shown in Fig. 11(b).[28]

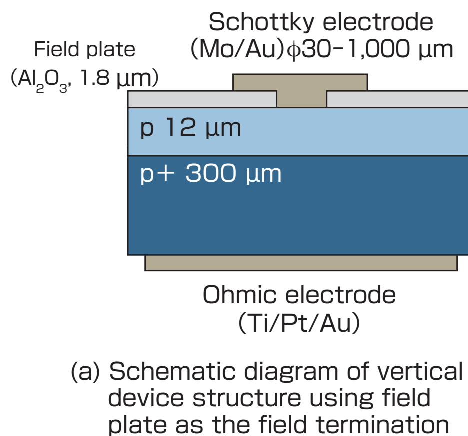
For the high-speed operation property, joint research was done with Professor Funaki of the Graduate School of Engineering, Osaka University. The switching characteristics of the diamond diode was measured, as the recovery of the diamond Schottky diode was measured using the “double pulse method” after constructing the driving circuit using the Si MOSFET. Figure 12 shows the switching property. This corresponds to (8) in the synthesiology tree in Fig. 3.

For the high-speed switching of (8), the high-speed switching of 0.01 μsec and small reverse recovery current (low loss) of 40 A/cm^2 were confirmed for the high-speed operation at 225 °C in small vertical diode that was our first prototype. The operation at 250 °C was achieved in a 1 A class device.[28][31]

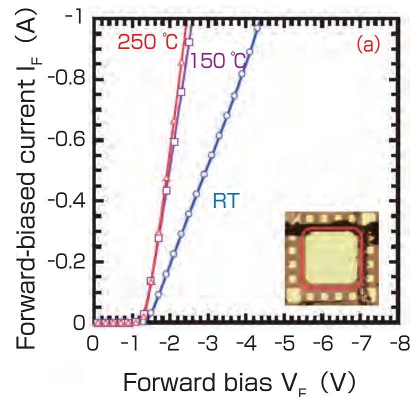
By demonstrating that the diamond diode could operate in high temperature at high speed and with low loss in a structure that is actually used, even in a small vertical device, it can be said that Phase 1 (superiority verification) of this research was cleared.

5 Future prospects and roadmap

First of all, the main issue is the growth of epitaxial film with low defects. While we were able to eliminate the killer defects, it is known that the leakage current increases significantly if the device size is increased,[32]-[34] and the most important issue is to decrease the defects. At present, we have started to work on identifying the defect types, effects on the device characteristics, and the ways to reduce them. The research from this perspective has not been done intensively for diamond, and it is necessary to return to basic research. Currently, through various analysis such as x-ray topography, the presence of edge dislocation and mixed type dislocation

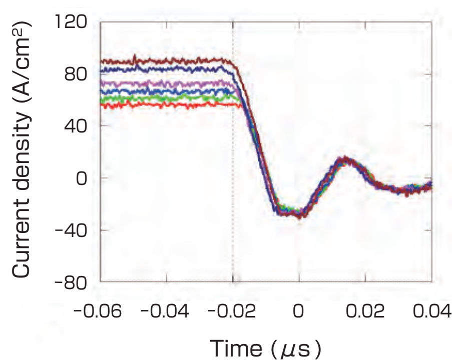


(a) Schematic diagram of vertical device structure using field plate as the field termination

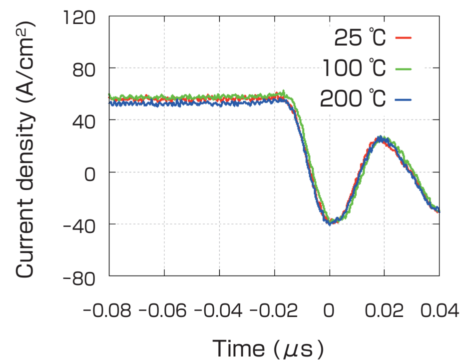


(b) Example of forward-biased property of diodes

Fig. 11 Ampere class diamond Schottky diode with field relaxing structure
(From Reference [28] H. Umezawa *et al.*)



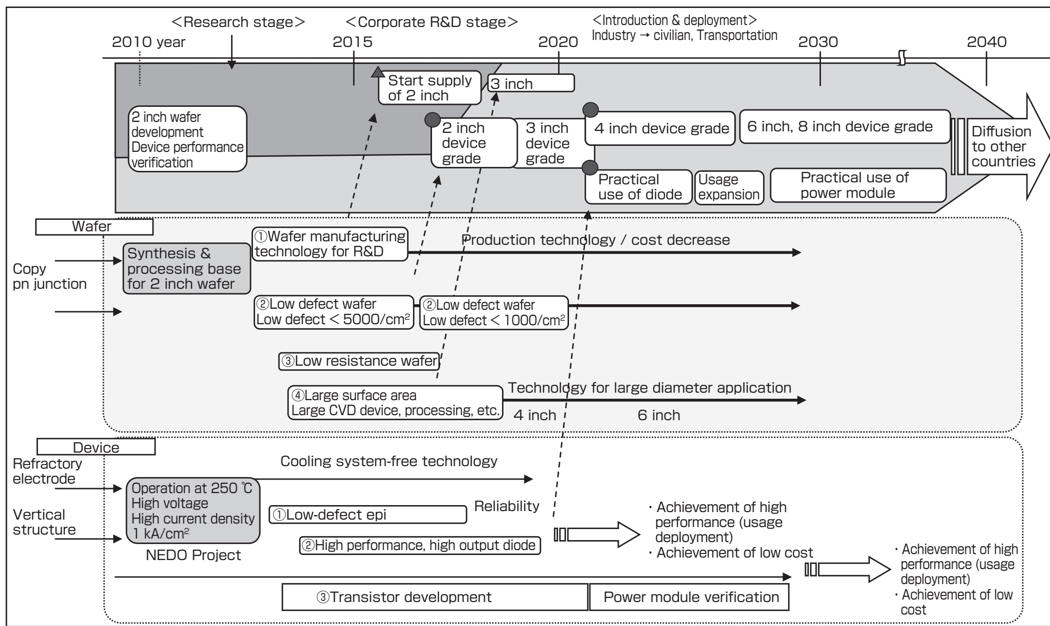
(a) Comparison at various current levels (show same high-speed recovery property)



(b) Comparison at various temperatures (show same recovery property)

Fig. 12 Recovery property of the diamond Schottky diode
(From Reference [29] K. Kodama *et al.*)

Table 1. Roadmap for the diamond power device and wafer



as main defect types and rough defect density are being discerned,[35][36] and detailed investigation of defects' influence to the device characteristics is being done. We aim to achieve the practical vertical structure device and the verification of several to 100 A devices.

For transistors, many researches have been studying diamond to achieve high speed and high frequency application using the lateral device structure.[37]-[39] However, vertical device structure with high breakdown voltage and high output current is mandatory for the power device, and it is necessary to speed up research based on past findings. We plan to investigate the superiority quantitatively, including the technology to achieve cooling free operation at high temperature through device implementation.

Table 1 shows the roadmap of the wafer and device created through surveying industry and academia, based on the technological strategy map of METI. For wafers, the supply system for 2-inch wafers is built jointly with companies to help promote the device research at the companies and universities. Also, the developments of practical wafers such as low-resistance and low-defect wafers are planned. For devices, the researches for low-defect epitaxial growth and

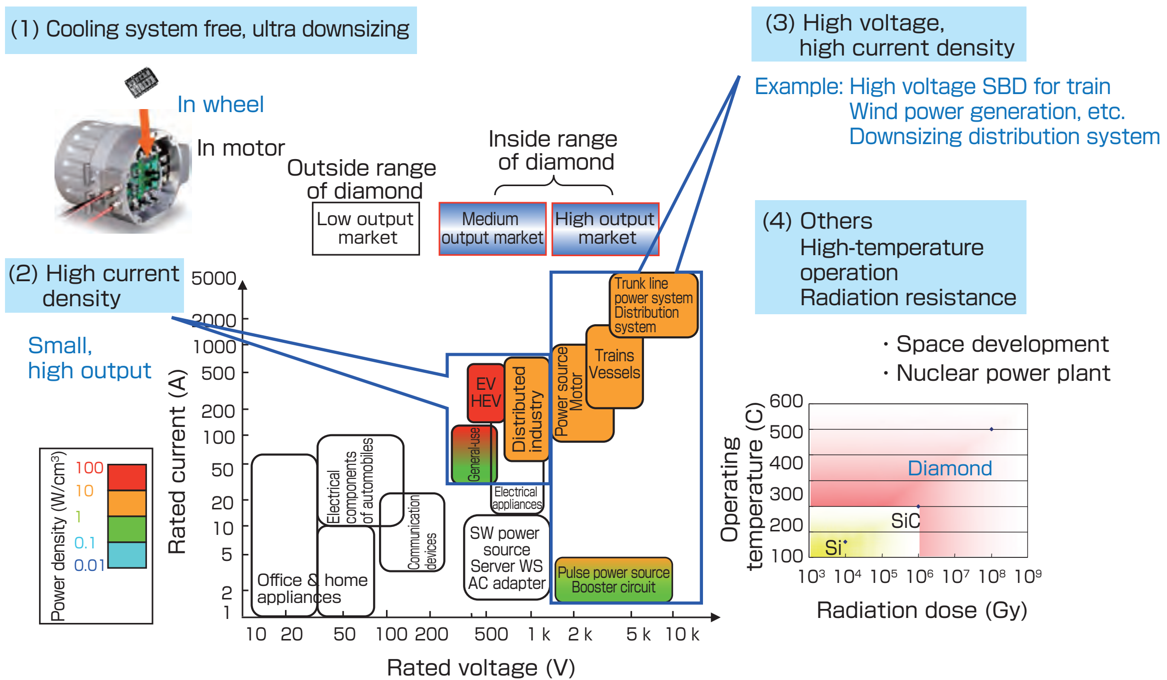


Fig. 13 Prospect of diamond power device application

others will be conducted toward the practical use of Schottky diode, to promote the practical utilization of high-output, high-performance diodes. At the same time, the research for MIS (MOS) type field effect transistors (FET) and pn junction transistors will be done jointly with several universities. As an application, development will be done with prospects in mind as shown in Fig. 13 through interviews with companies.

We have just started the *Full Research* that may require a long time. However, we wish to speed up the development to enable this material to become the main material and device of the 21st century, to meet the national interest of Japan in terms of resource and safety, and also to help solve the issue of global warming.

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Note) http://www.enecho.meti.go.jp/policy/coolearth_energy/coolearth-hontai.pdf

Terminologies

Term 1. Field relaxing structure: The structure of the device is made to maintain breakdown voltage by dispersing and avoiding the concentration of electric field. Field plate and junction termination structures are well known.

Term 2. Drift layer: This is the active layer that operates as the power device.

Term 3. Vertical structure and pseudo vertical structure: Since large current flows through the power device, the current is led through the whole surface using a structure with vertical current route, rather than through a lateral structure device used in LSI and high-frequency devices. The pseudo vertical device is a test device with insulated substrate, and only its active layer is vertical, while the extraction of current is done from the top. See Fig. 3.

Term 4. Themionic field emission (TFE) model: Of the three models of carrier conduction in the Schottky barrier junction, this model incorporates both the effects of thermo electron and field emission.

Term 5. Avalanche breakdown: The phenomenon that leads to destruction as massive current flows like an avalanche, as free electrons are accelerated in the field and collision ionization occurs repeatedly.

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Discussions with Reviewers

1 General

Question and comment (Naoto Kobayashi, Center for Research Strategy, Waseda University)

This paper reports the results of the comprehensive research for superiority verification of diamond used in power semiconductor devices. It presents the general outcomes starting from the individual elemental technology that the authors have accumulated over the years to the actual verification, and it is a significant paper to be published in *Synthesiology*. Particularly, I think it can provide an effective guideline and direction to readers who may be working on the practical utilization and realization of diamond power devices. However, there are ambiguous expressions that are somewhat difficult to understand, and careful revision is necessary.

Question and comment (Toshimi Shimizu, AIST)

This research shows the result of the superiority verification of next-generation power semiconductor device that uses diamond materials which possess optimal performance among several substances. Its content is equivalent to *Full Research* as the four synthesis elements were solved along with the reference to breakthroughs. It is indeed appropriate as a *Synthesiology* paper. Although there is no major problem in the logical composition, I think you need to work on making it more understandable to the general reader. If this point is supplemented, it will be a more satisfying paper.

2 Research scenario and specific application

Question and comment (Naoto Kobayashi)

Figure 3 shows the scenario (synthesiology tree diagram) for the superiority verification research of diamond power devices. This is the important main focus of this paper in terms of synthesiology. However, the meaning of the numbered items such as (1) electrical breakdown, (2) killer defect elimination, etc. and their relationships are hard to understand. There are some explanations in chapter 4, but it is unclear whether they show the passage of time or the order of research conducted, and you need some explanation in the text or in the caption of the figure.

Answer (Shinichi Shikata)

The numbers indicate the order in which the researches were ultimately conducted. I added a note in the figure. They more or less follow the basic plan that was created in December 2004, and combined with the wafer development for which the research was done concurrently, they lead up to the roadmap shown in Table 1. The future issues are the breakthroughs needed for practical use as shown in the upper left of Fig. 3, and we hope to accomplish them in Japan with cooperation from various organizations.

Question and comment (Naoto Kobayashi)

There is a brief description of the application of diamond power devices in chapter 1. Since this is the most important part for enabling practical use of the results of this paper, I recommend that it be discussed in detail by using a diagram (such as that you have shown on http://www.chubu.meti.go.jp/jisedai_jidoushiya/chiubu/pdf/sansoken/sansoken_8.pdf), which will help the readers' understanding.

Answer (Shinichi Shikata)

I added the figure that I left out due to space limitations. I added the names of specific application devices. In the ENERGY OUTLOOK of IEA, 67 % of the CO_2 reduction is accomplished by energy-saving technology, and I wish to attain practical use as soon as possible to meet this demand. Looking at the example of SiC, the Schottky diode that we took up as an exemplary device in this paper has more merit compared to the Si pn diode, and I think there is good possibility for the medium output devices. Also, diamond has excellent resistance to gamma rays and neutron rays, and I think there is potential in small current devices.

3 Comparison of the performances of low-loss power devices and status of the R&D of the diamond device

Question and comment (Toshimi Shimizu)

You compare various property values for substances including diamond, SiC, GaN, and Si, but I would like to know the benchmark information of the devices to which such substances are actually implemented. In other words, in future power device applications, how will diamond exert its characteristics? What are the evidences and reasons for such claims? Please describe them. In the *Synthesiology* paper written by Kazuo Arai, "R&D of SiC semiconductor power devices and strategy towards their practical utilization - The role of AIST in developing new semiconductor devices" [*Synthesiology English edition*, Vol. 3, No. 4, p. 245-258 (2011)], there is a conceptual diagram that clearly shows the relationship between the application of power semiconductor and device performance in demand (p. 256). For easier understanding, I think you need to create a similar figure by superimposing the performance of diamond on this diagram.

Answer (Shinichi Shikata)

I created a new figure. I showed the specific applications according to the categories of current and voltage. In fact, by adding the cooling free and high temperature axes, it shows the characteristic merit of diamond that can be used without decreasing output.

Question and comment (Naoto Kobayashi)

In this paper, there are detailed explanations of the content and significance of the elemental technologies that the authors have accumulated over the years, but there is no explanation on the ongoing R&D in Japan and overseas, and this gives an obscure impression of the positioning of this research. I hope you address other R&Ds such as, for example, T. Iwasaki *et al.* [*Appl. Phys. Express*, 5, 091301 (2012)]. You should also cite the patent information, since your results have been utilized as patents.

Answer (Shinichi Shikata)

I added the prospects by citing the papers on transistors. The recent paper that you indicated is a research on the device based on pn junction, and ultra high breakdown voltage is assumed for its use. However, over 10 order improvement from nA to 100 A class is needed. In diamond, n+ doping has not been achieved, and further material research is necessary. Currently, I think the unipolar device that can be driven at low voltage will take the

lead, just as it happened in SiC. Since the device in this paper is already 1 A class, we are aiming for double-digit increase by reducing the defects. For patents, there are several that have been registered including the patent unique to diamonds.

4 Advantage verification

Question and comment (Toshimi Shimizu)

At the end of “1 Objective and outcome of research,” you write, “Phase 1 of R&D was conducted to verify the advantage….” For example, drug discovery starts from basic research, nonclinical trial using animals, and clinical trial in humans to see the efficacy and safety of the drug (Phase 1~3). Here, there is a giant difference between the research phases of whether the subjects of verification are animals or humans. In device research, what is the major synthesis element or technological element that separates Phase 1 research for concept verification and Phase 2 for practical device verification, as shown in Fig. 3? Is it a difference perceived by the author, or is it a generally accepted difference? Even if it is common sense to device researchers, the positioning of Phase 1 and 2 is not clear to the general readers.

Answer (Shinichi Shikata)

The concept verification of Phase 1 is an animal experiment in the sense that confirmation is done, for example, at 1 A class for whether the principle is realizable or not. The device development of Phase 2 is an efficacy check in humans in the sense that it is verification of 100 A class that can be actually implemented. The reliability test is Phase 3 or the safety test. After this, the phase proceeds to engineering samples and products. Although the names are different by companies, this is a common concept. I added supplementary explanation in Fig. 3.

5 Performance verification of transistor

Question and comment (Toshimi Shimizu)

To aim for power device verification using the diamond semiconductor, I think the verification of not only diode but also transistor performance is essential. Recently, there was a paper published by an AIST research group about the success of verification of operating junction type field transistor for the first time. Your paper does not address the future prospect of transistor operation using the diamond semiconductor. If you are aiming for an ultimate power device, I think you must comment on the latest technological trend on the transistor development using diamond materials.

Answer (Shinichi Shikata)

There are mountains of trial results from way back, but unfortunately they involve only the lateral structure device that aims for high frequency, and there is no success with prototypes with vertical structure that may lead to the future 100 A class. However, as you say, there is a lack of reference to transistors in this paper, so I added some comments. I think this item must be studied with the participation of multiple organizations.